

Compal Confidential

KAW60 Schematics Document

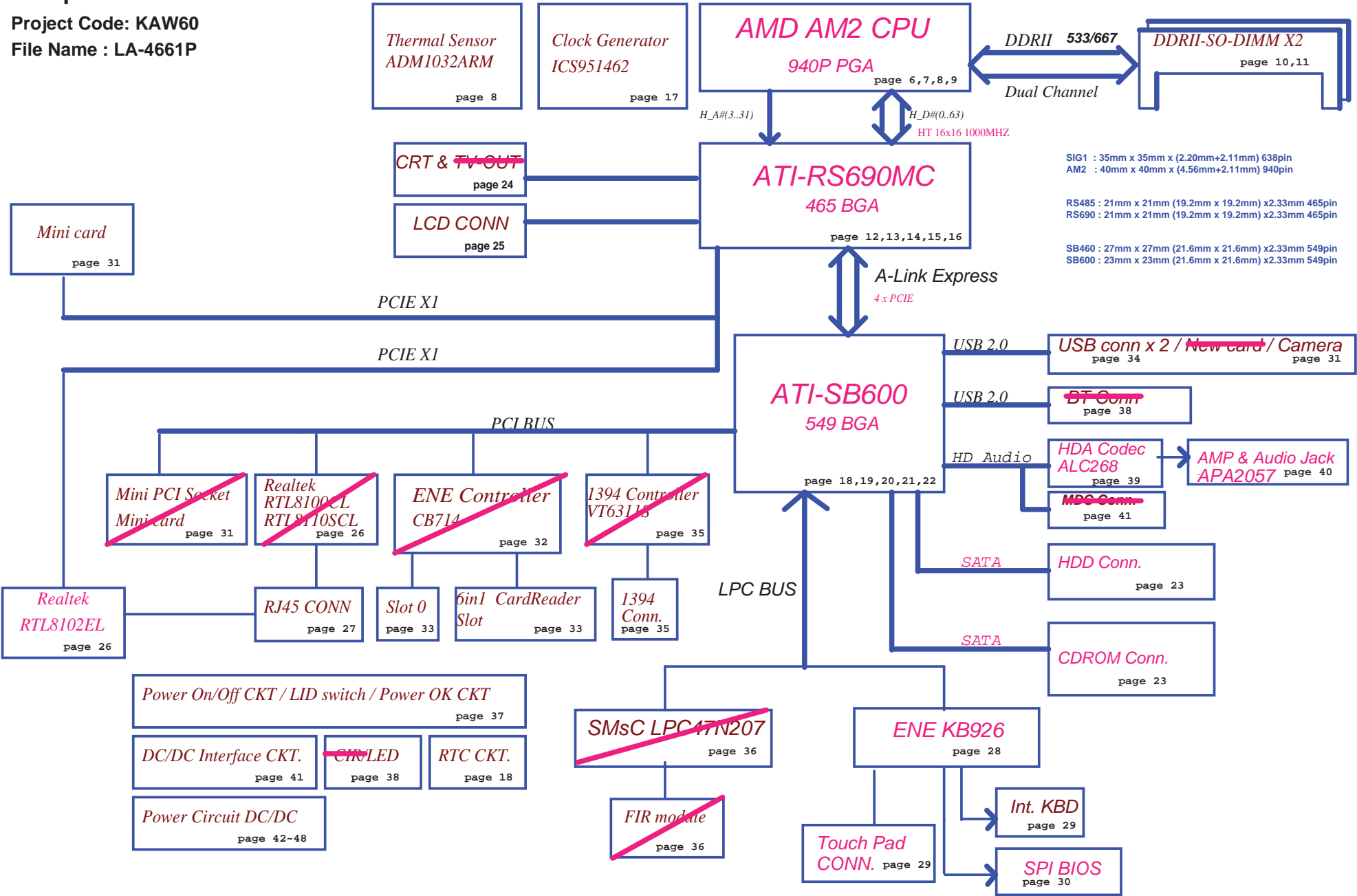
AMD AM2 / RS690MC / SB600

2008 / 07 / 25 Rev:0.2 FOR PVT

Security Classification		Compal Secret Data			
Issued Date		2005/05/09	Deciphered Date		2006/03/08
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				Cover Sheet	
				Size Custom	Document Number KAW60 LA-4661P
				Date	Friday, July 25, 2008
				Sheet	1 of 50
				Rev	2.0

Compal confidential

Project Code: KAW60
File Name : LA-4661P

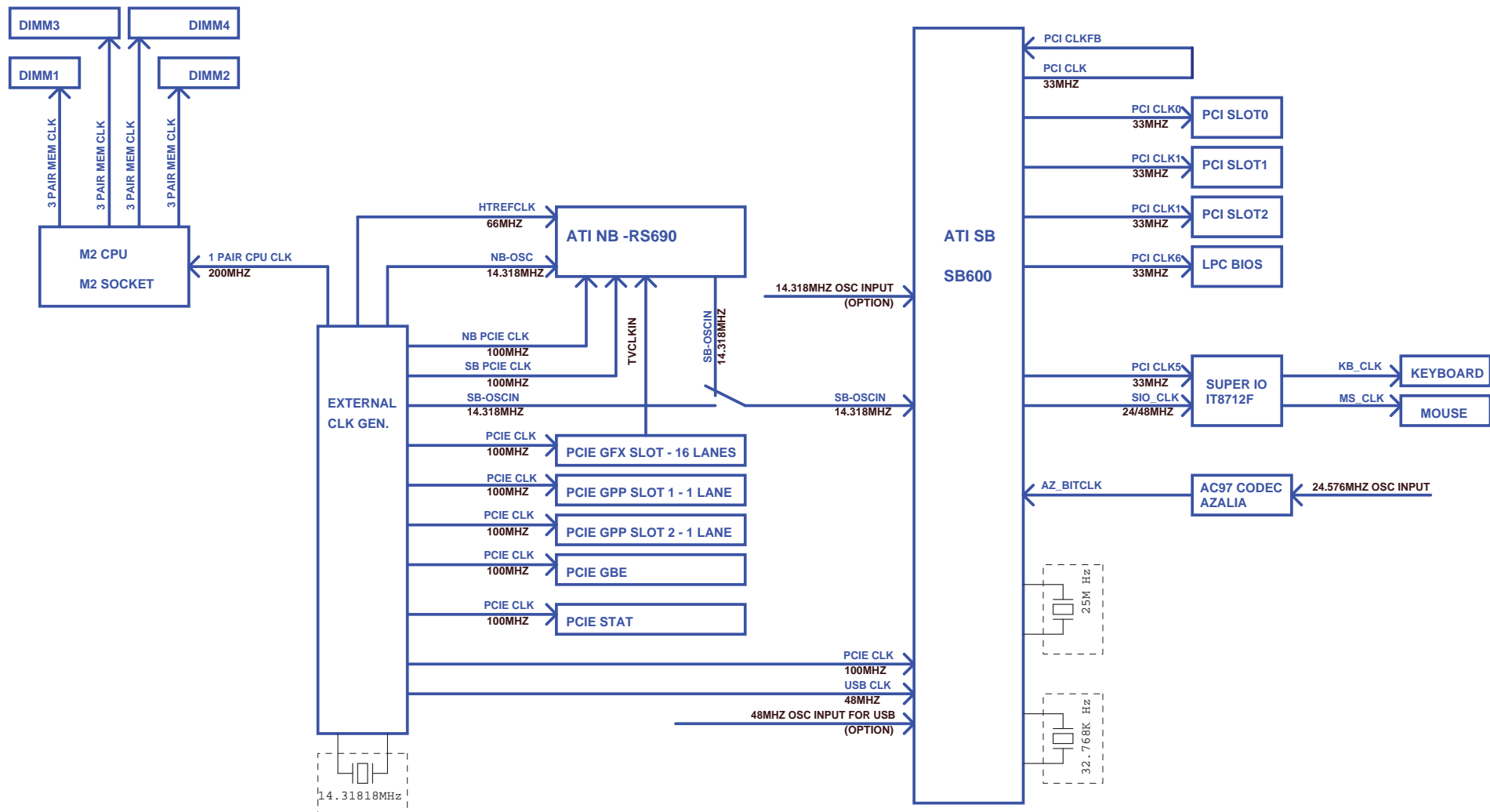


SIG1 : 35mm x 35mm x (2.20mm+2.11mm) 638pin
AM2 : 40mm x 40mm x (4.56mm+2.11mm) 940pin

RS485 : 21mm x 21mm (19.2mm x 19.2mm) x2.33mm 465pin
RS690 : 21mm x 21mm (19.2mm x 19.2mm) x2.33mm 465pin

SB460 : 27mm x 27mm (21.6mm x 21.6mm) x2.33mm 549pin
SB600 : 23mm x 23mm (21.6mm x 21.6mm) x2.33mm 549pin

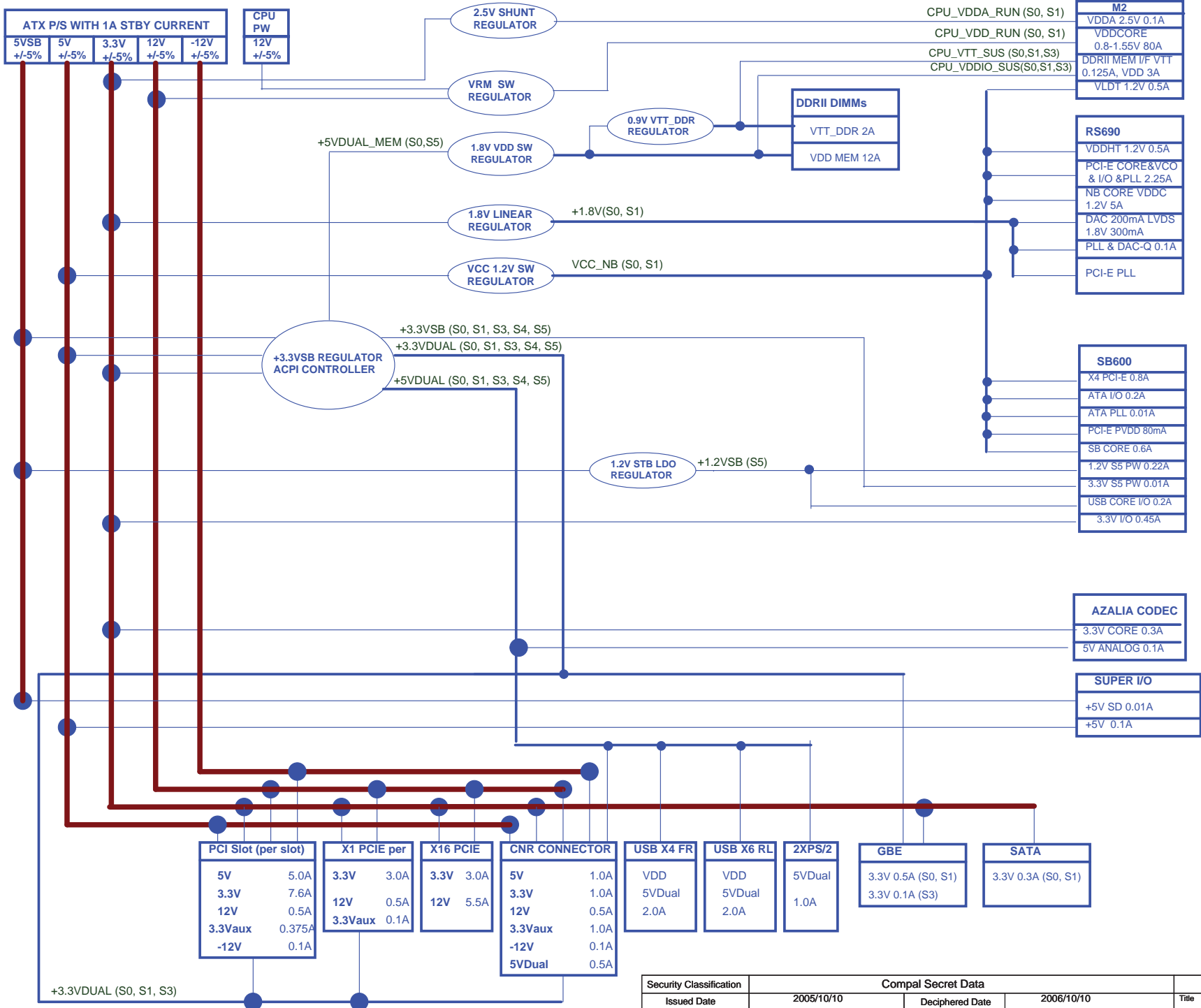
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	BLOCK DIAGRAM	
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ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

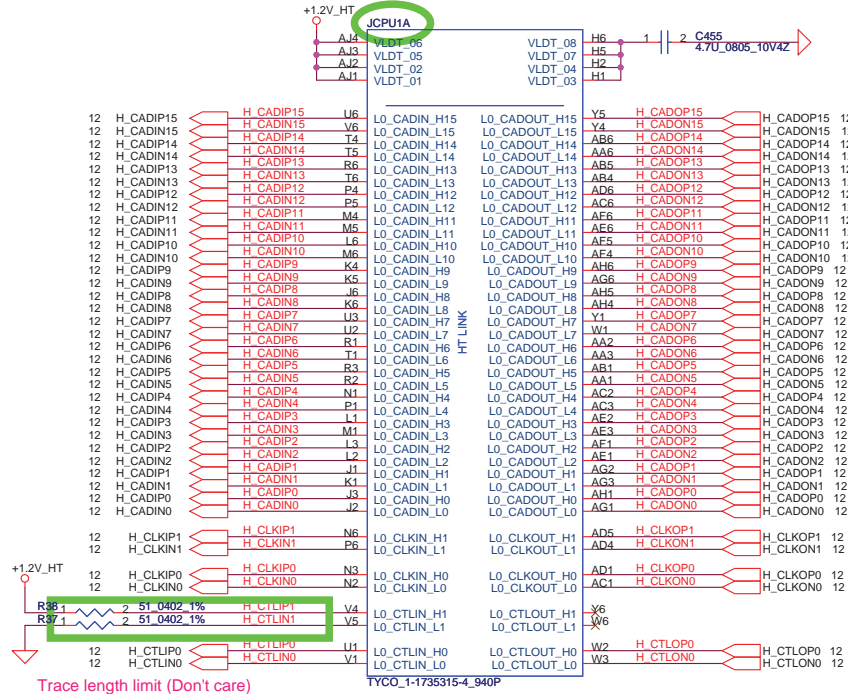
CPU PW
12V +/-5%



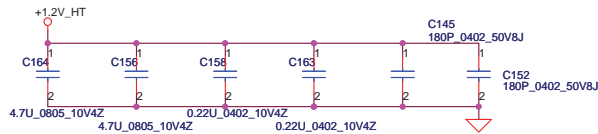
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PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



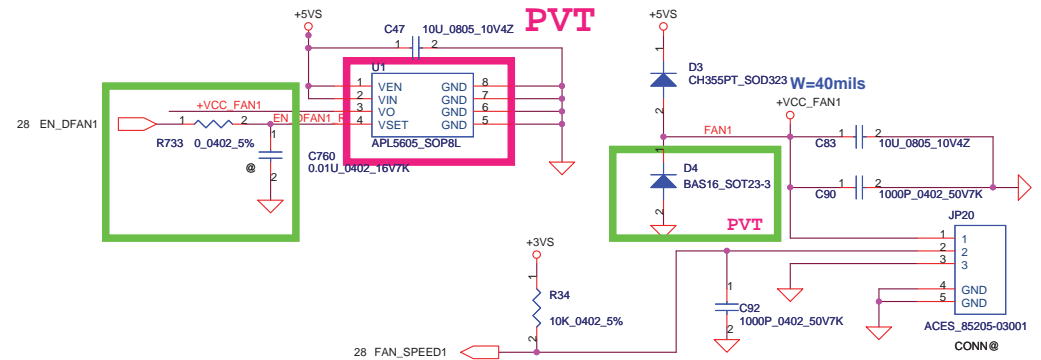
CONN@
SOC127MM48X51-948! 6090022000; JCPU1
TEMP SYMBOL



LAYOUT: Place bypass cap on topside of board

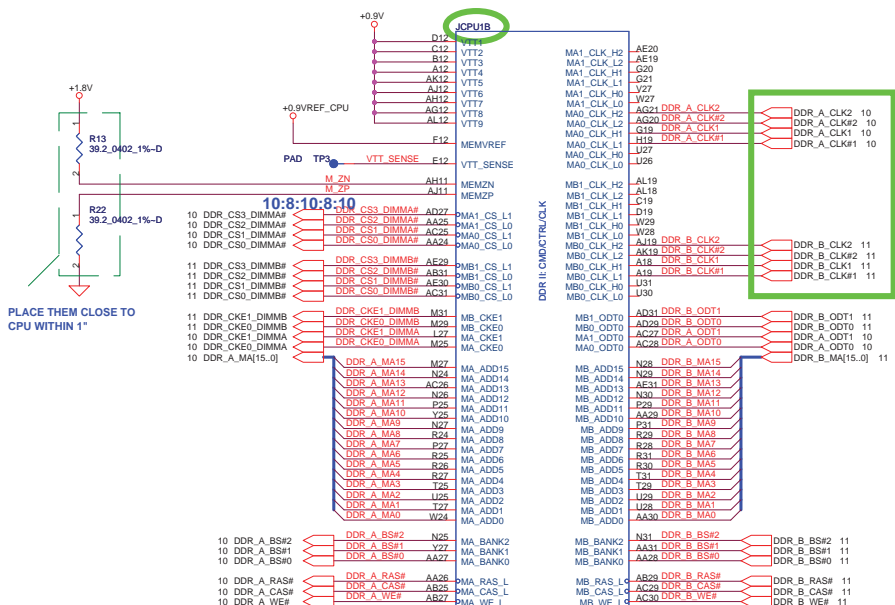
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS

FAN Conn

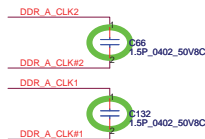


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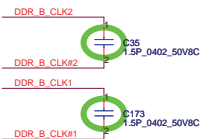
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



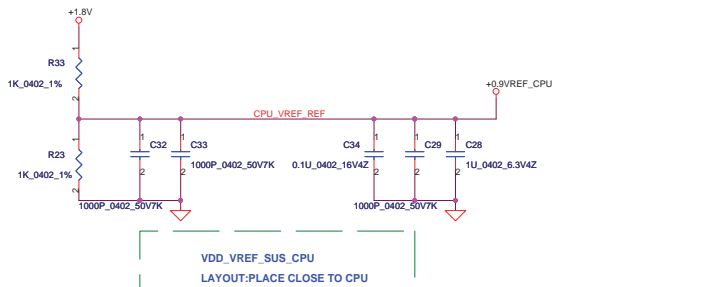
PLACE THEM CLOSE TO
CPU WITHIN 1"



PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH

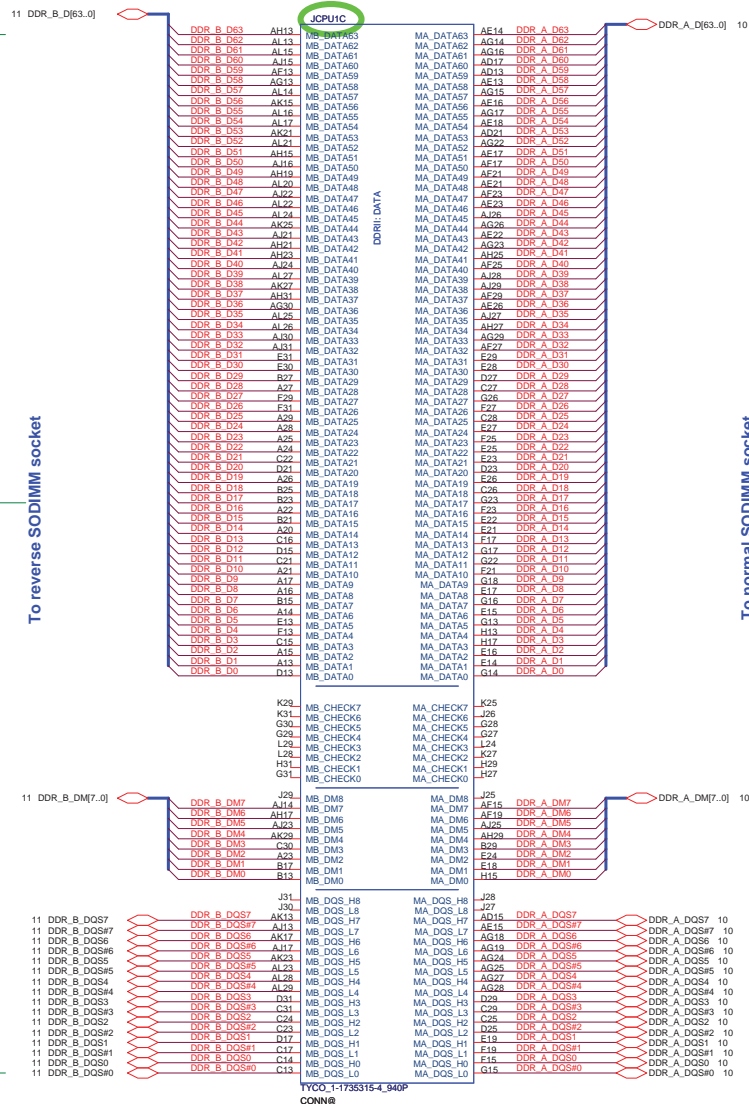


**PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH**



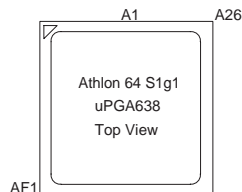
VDD_VREF_SUS_CPU

Processor DDR2 Memory Interface



To reverse SODIMM socket

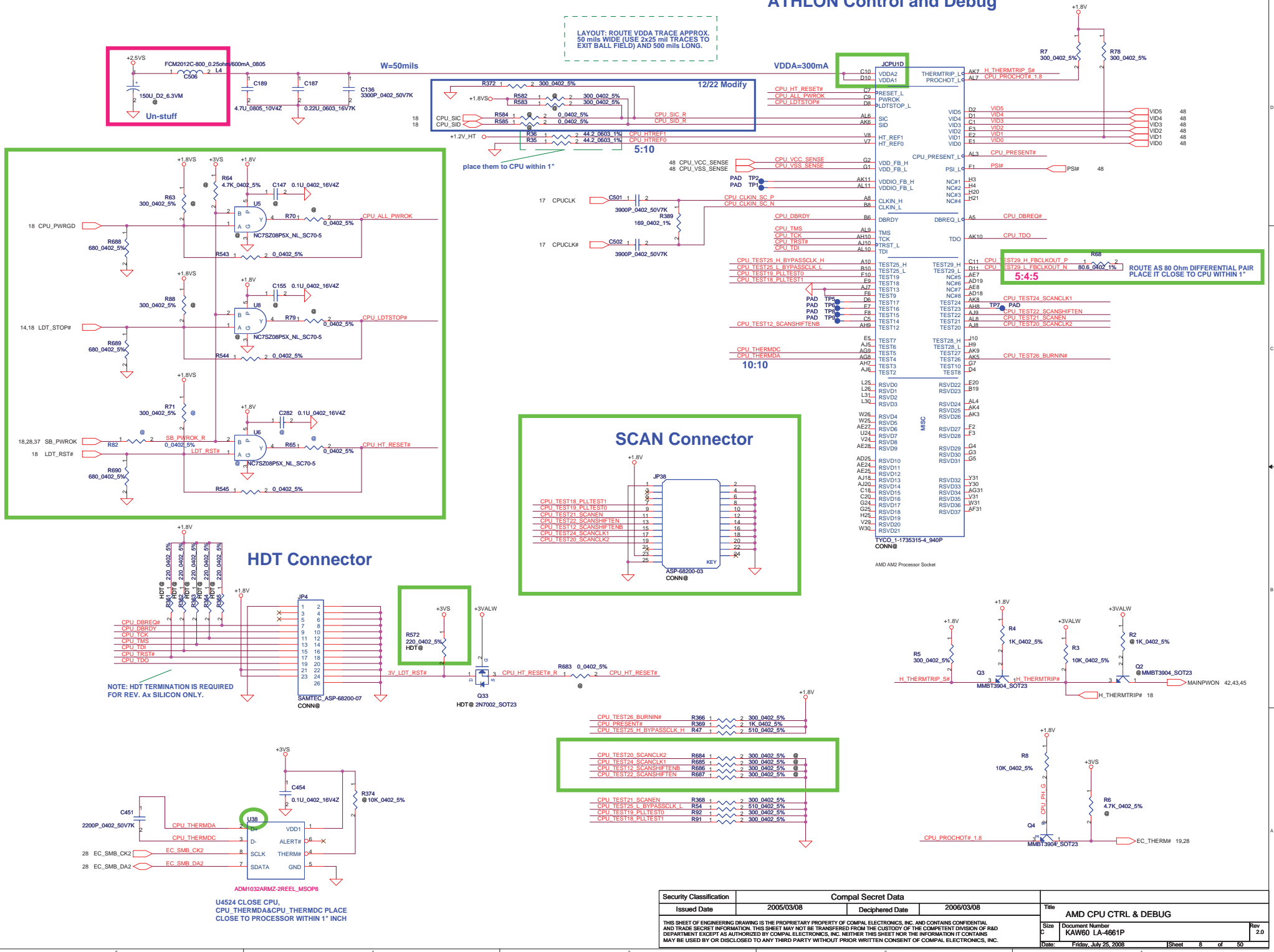
To normal SODIMM socket

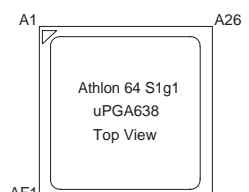
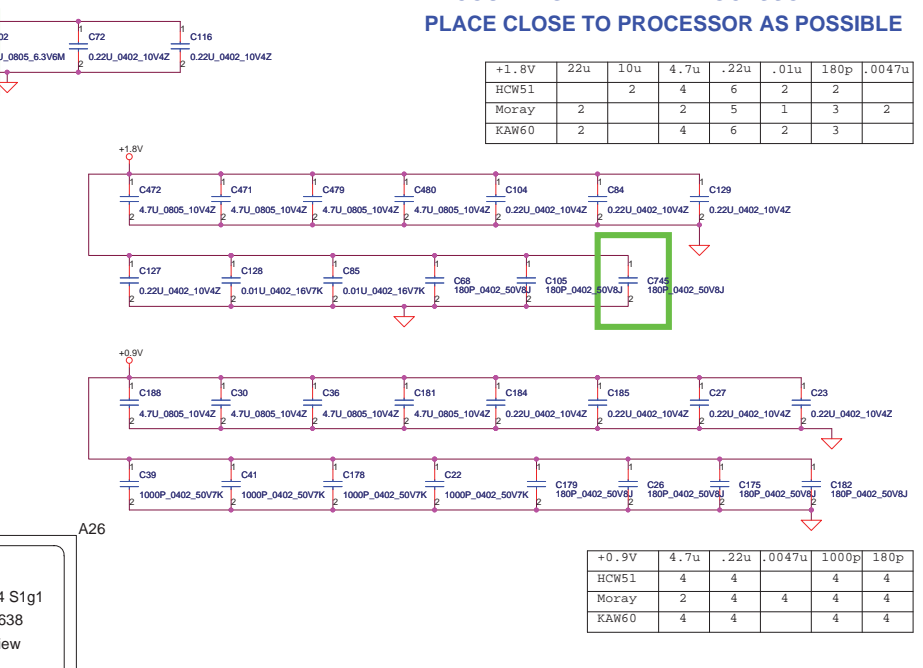
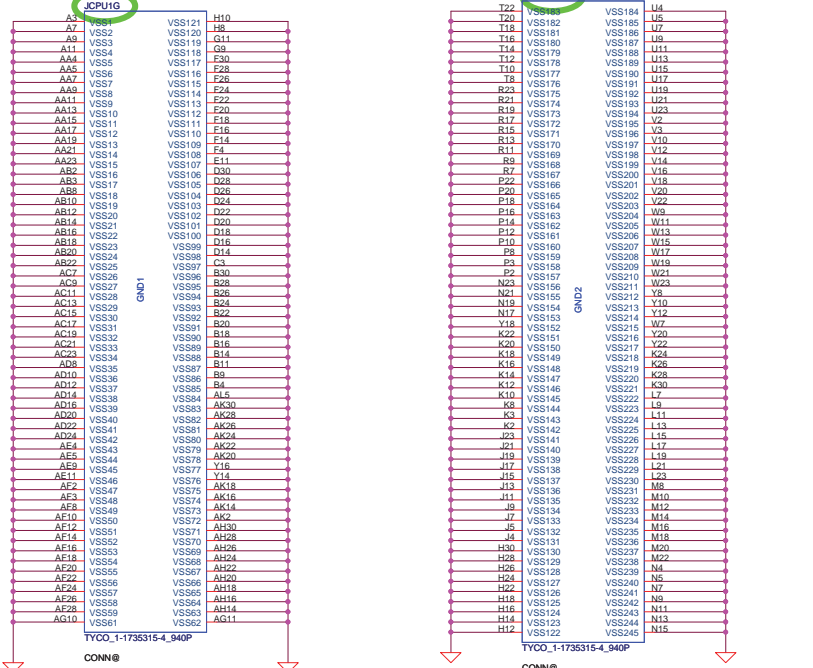
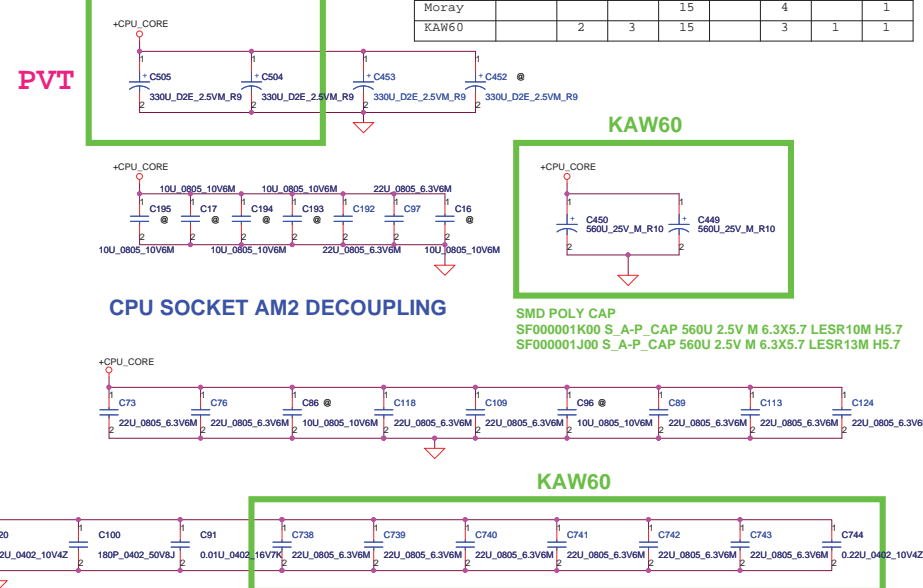
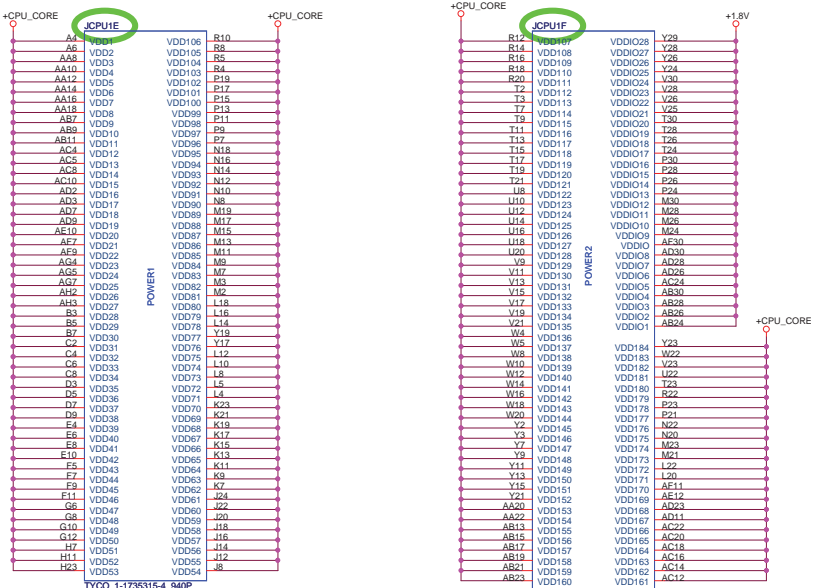


Athlon 64 S1g1
uPGA638
Top View

Security Classification	Compal Secret Data			Title	AMD CPU DDRII MEMORY I/F		
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ATHLON Control and Debug





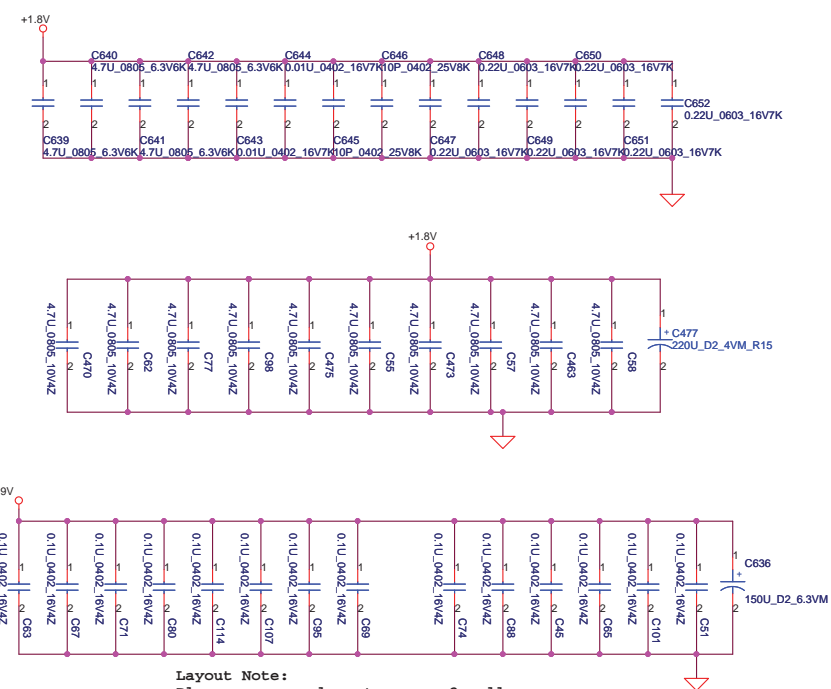
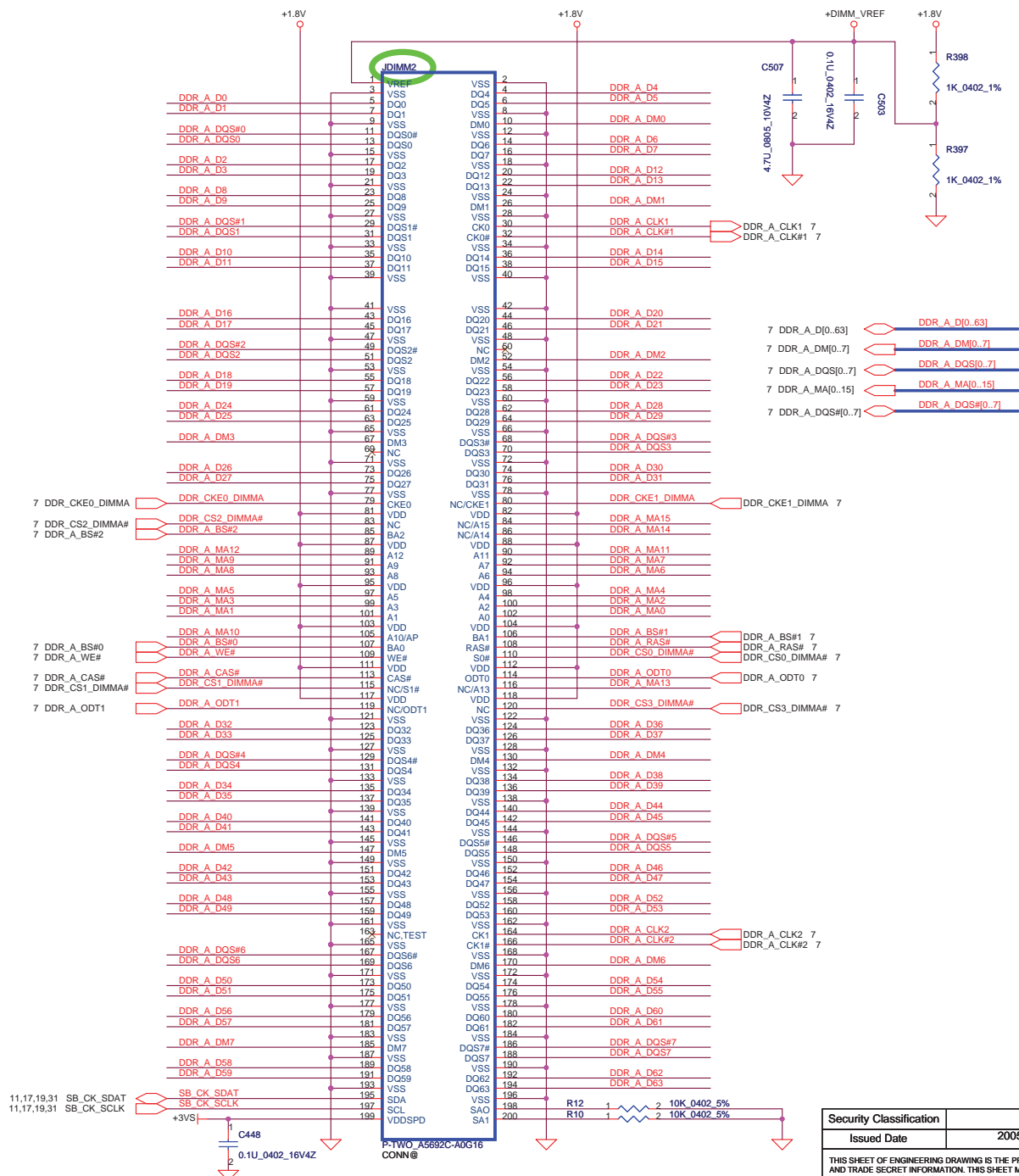
PROCESSOR POWER AND GROUND

	CPU_CORE	820u	560u	330u	22u	10u	.22u	.01u	180p
HCW51	2		2	4	12	2	1	1	
Moray				15		4		1	
KAW60			2	3	15		3	1	1

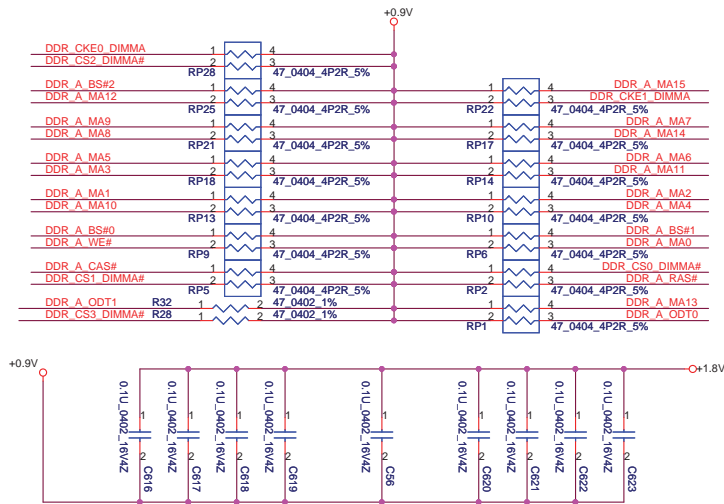
	+1.8V	22u	10u	4.7u	.22u	.01u	180p	.0047u
HCW51			2	4	6	2	2	
Moray	2		2	5	1	3	2	
KAW60	2			4	6	2	3	

	+0.9V	4.7u	.22u	.0047u	1000p	180p
HCW51	4	4			4	4
Moray	2	4	4		4	4
KAW60	4	4			4	4

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								Size		
								Document Number		
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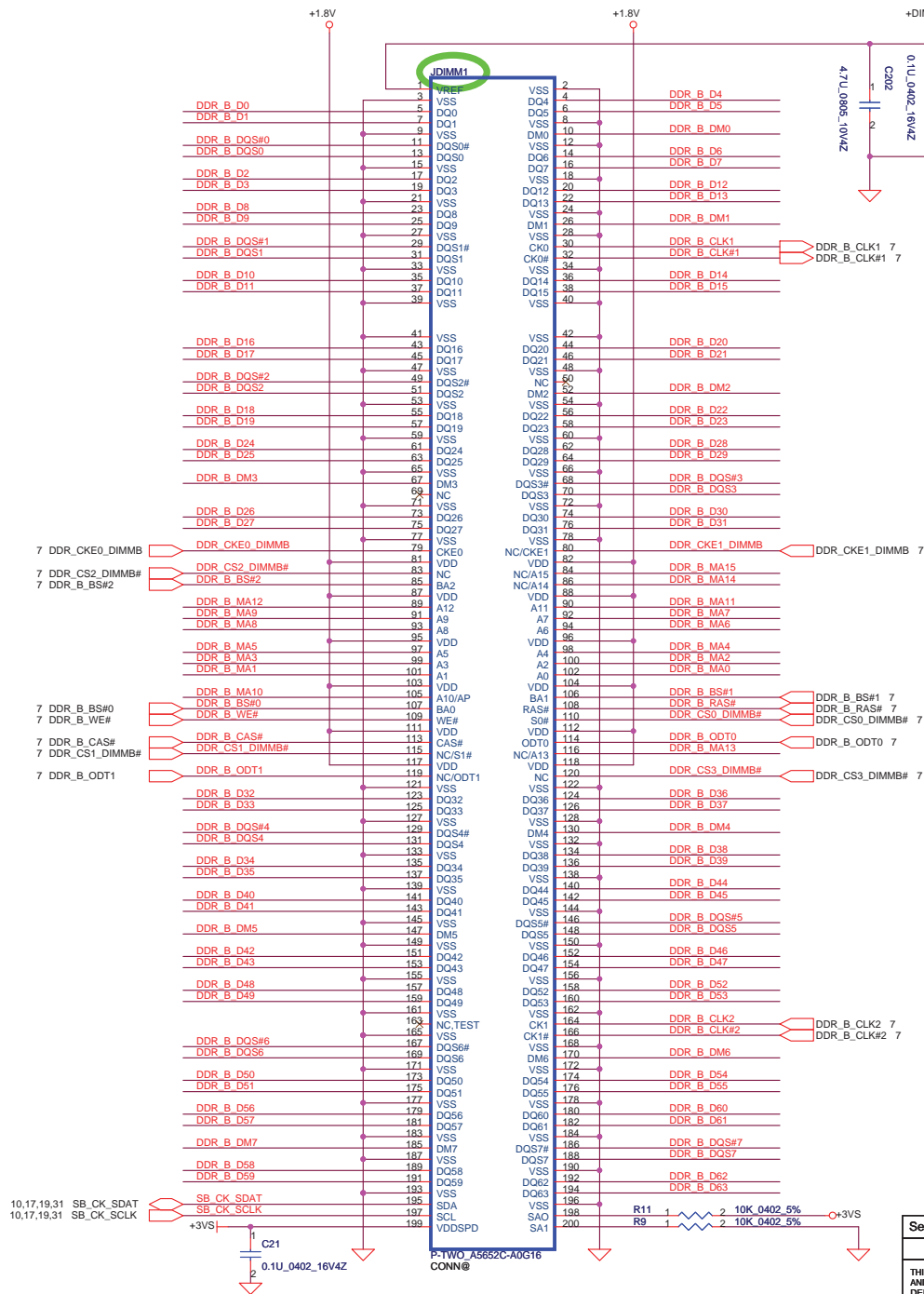


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

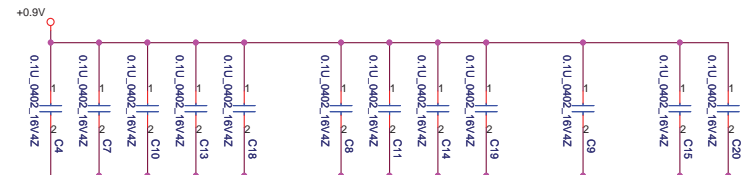
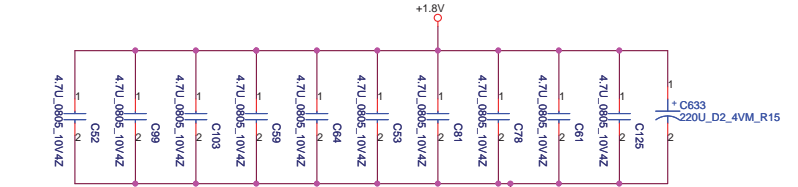


Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

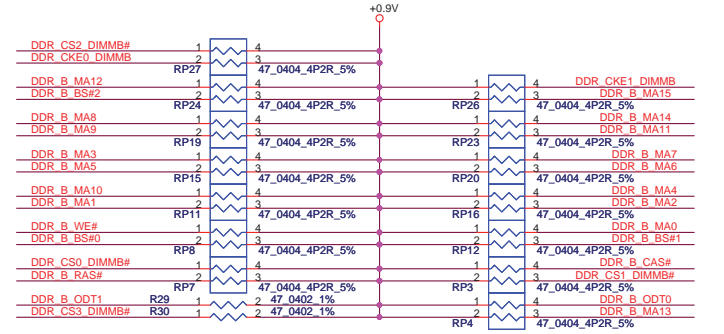
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- 7 DDR_B_D[0..63]
- 7 DDR_B_DM[0..7]
- 7 DDR_B_DQS[0..7]
- 7 DDR_B_MA[0..15]
- 7 DDR_B_DQS[0..7]

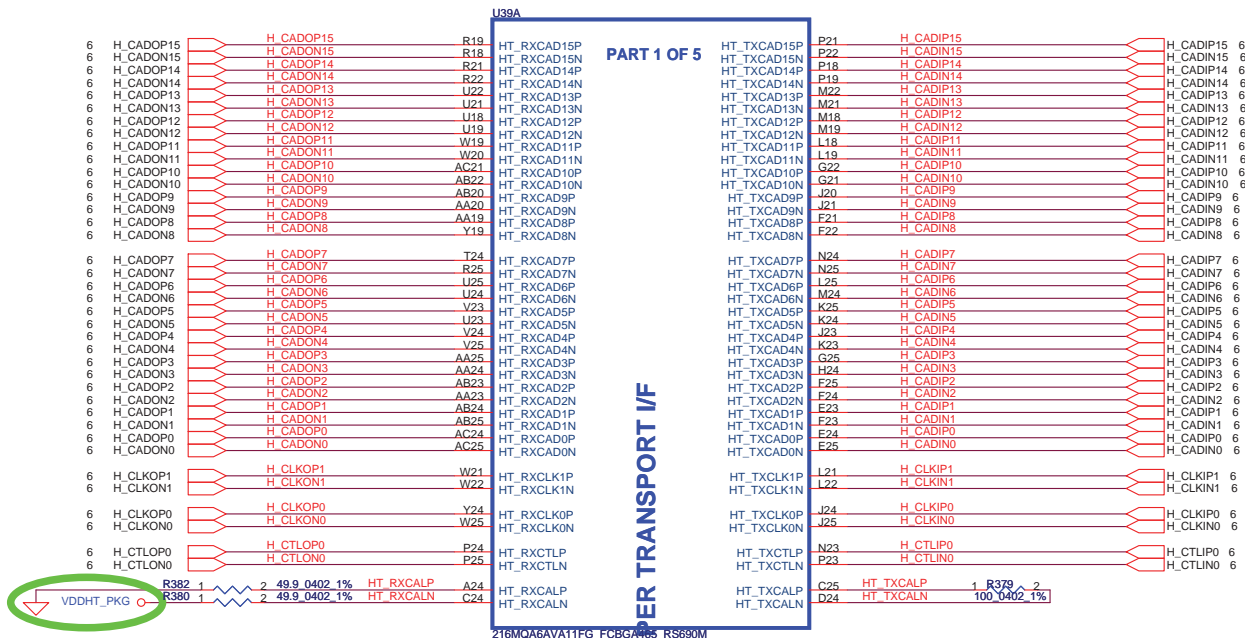


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

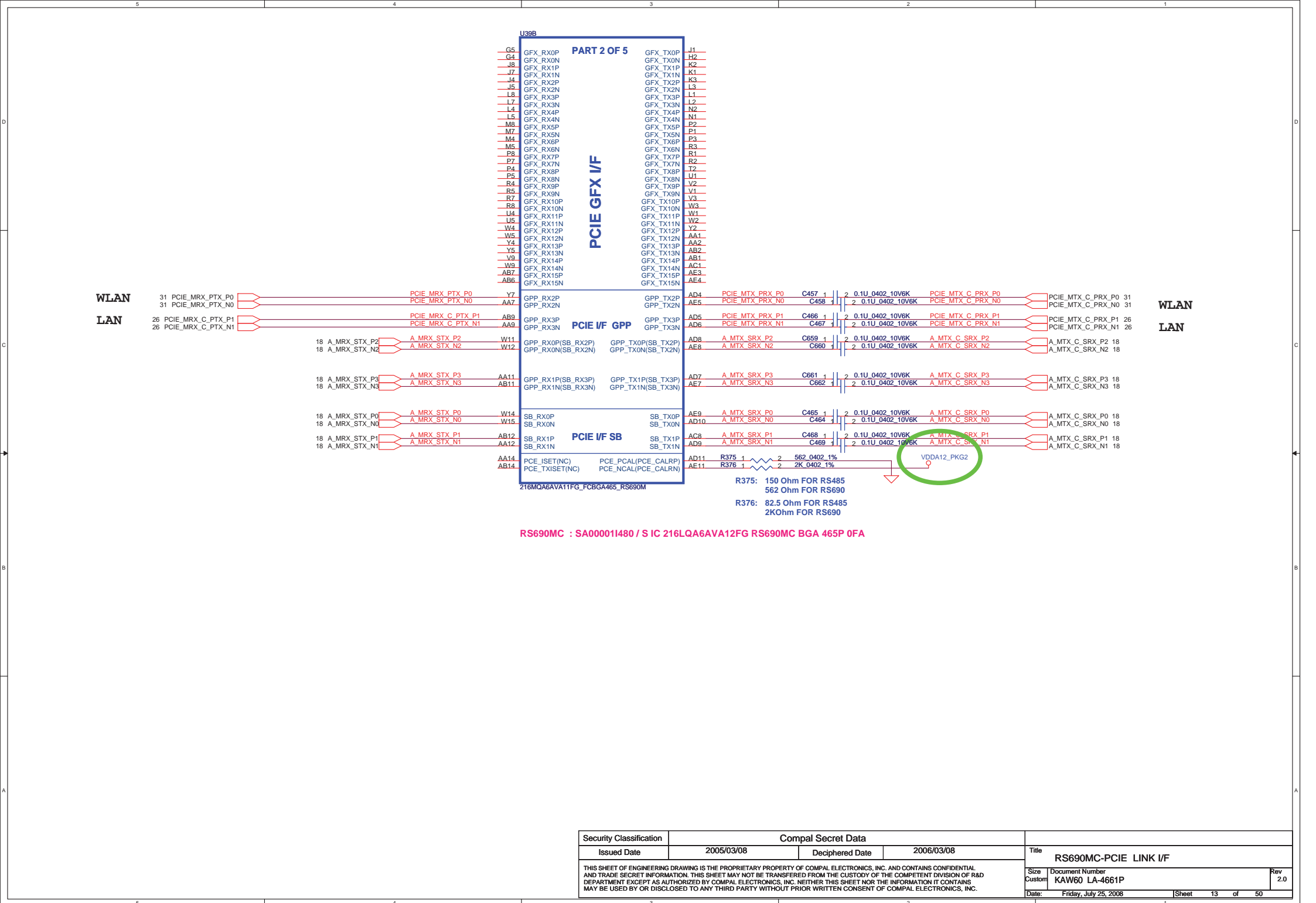


Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

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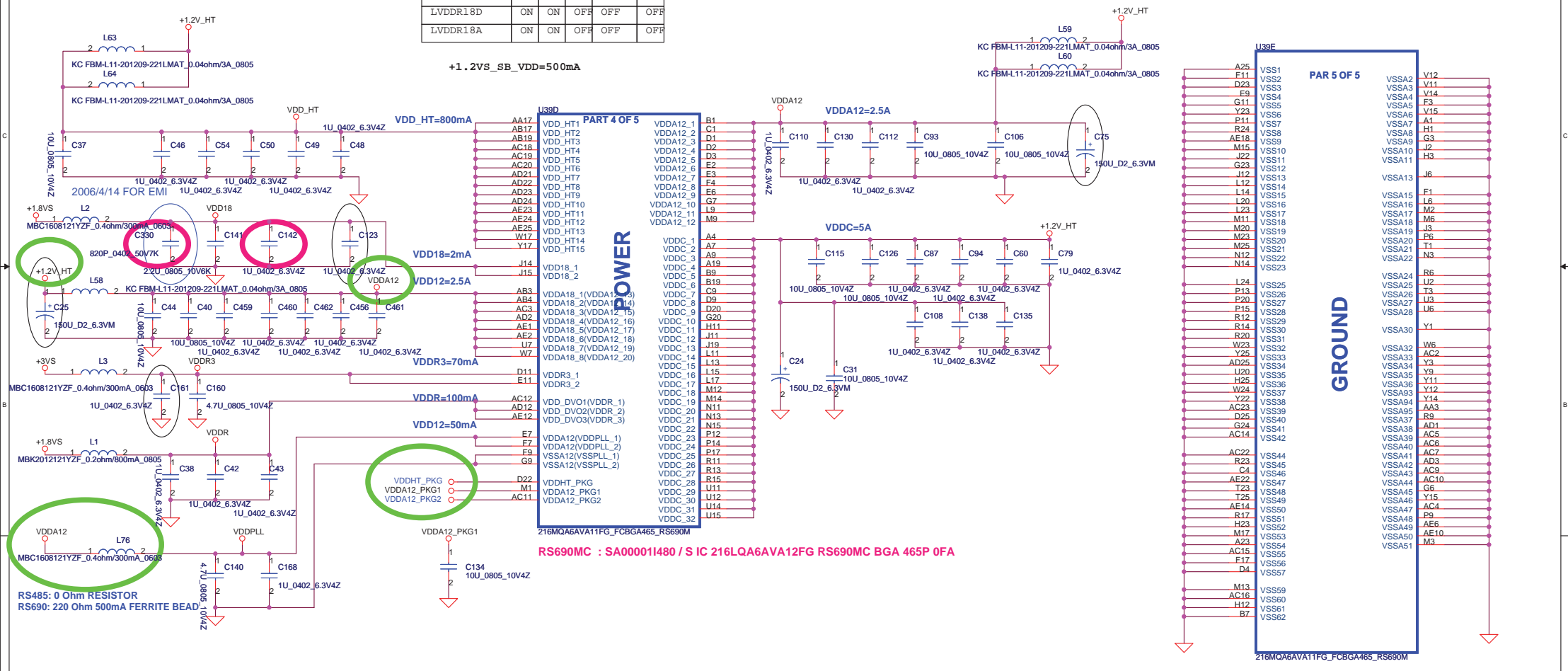
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NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

+1.2VS_SB_VDD=500mA

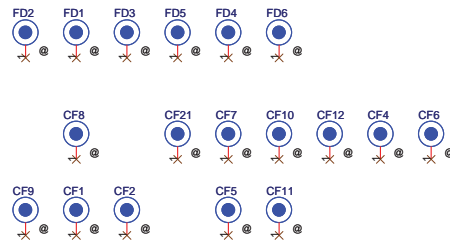
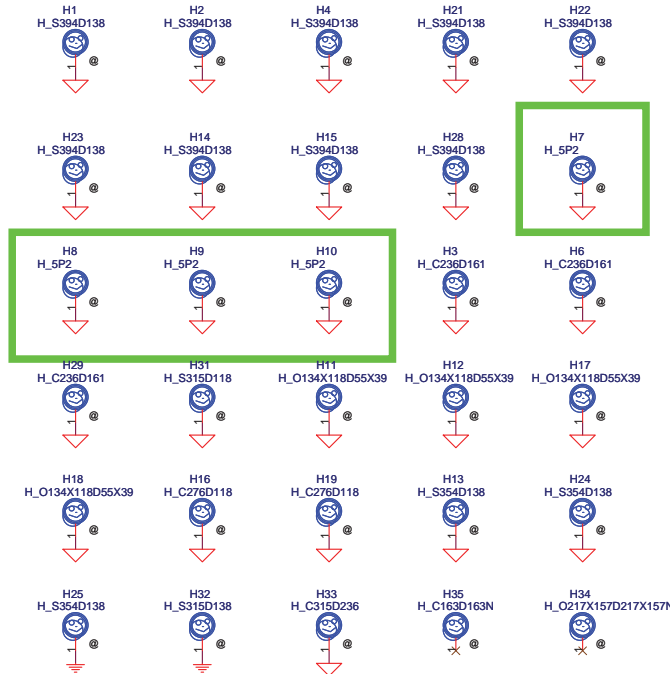
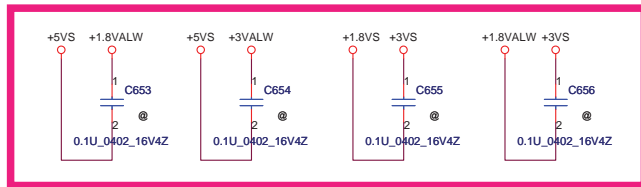


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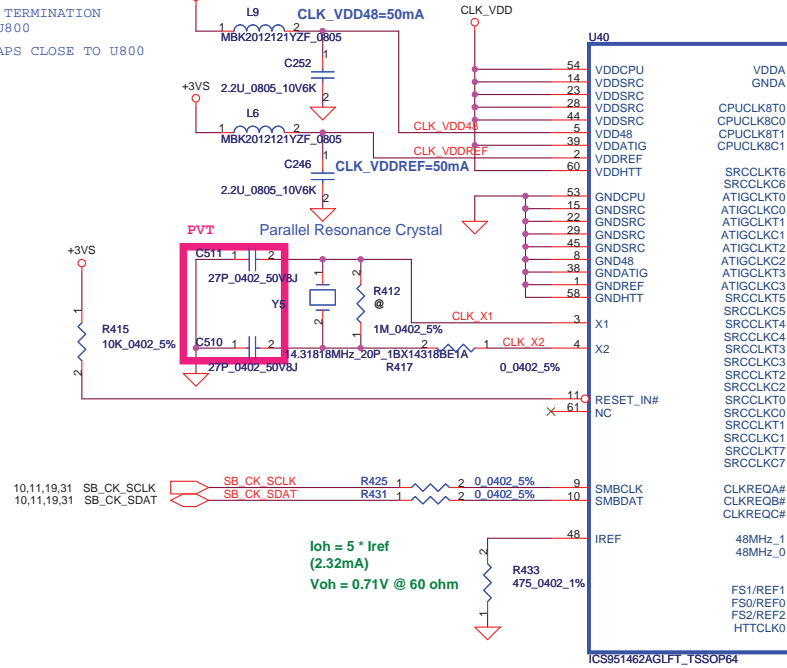
LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



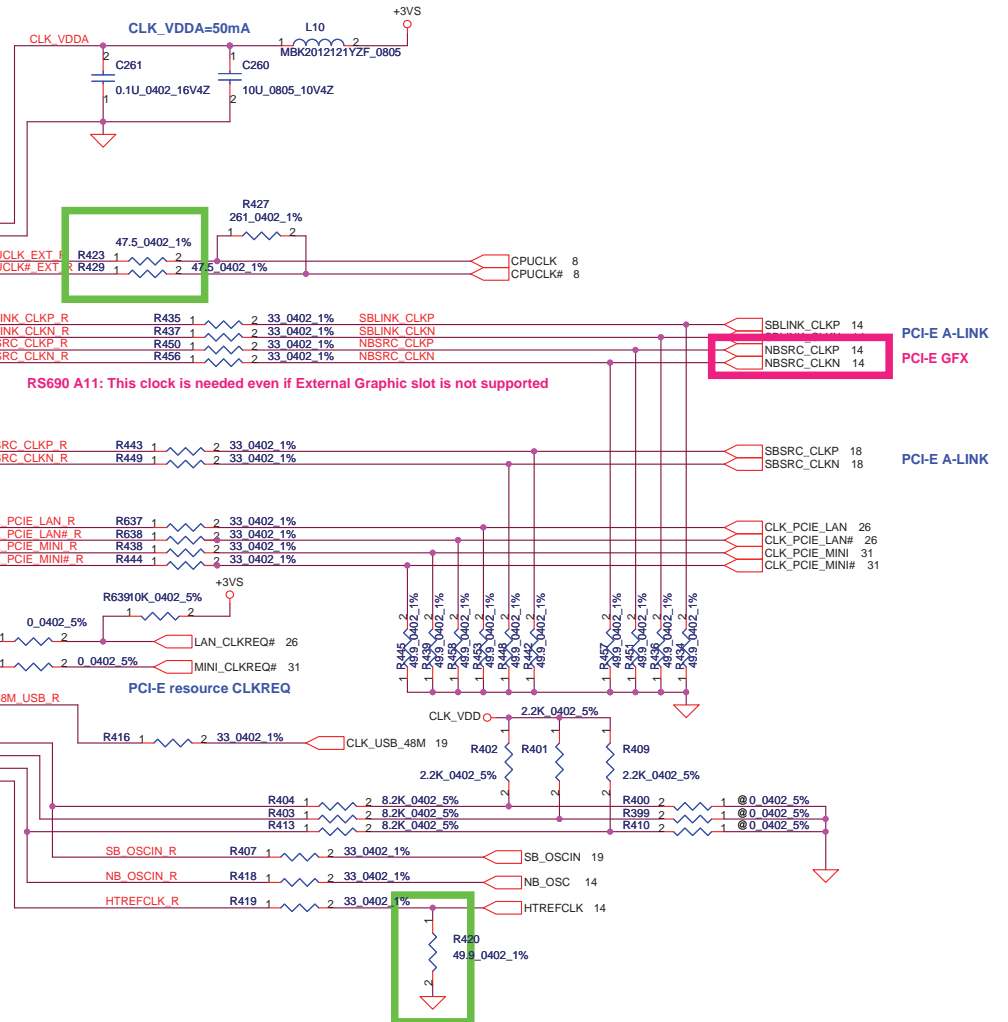
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

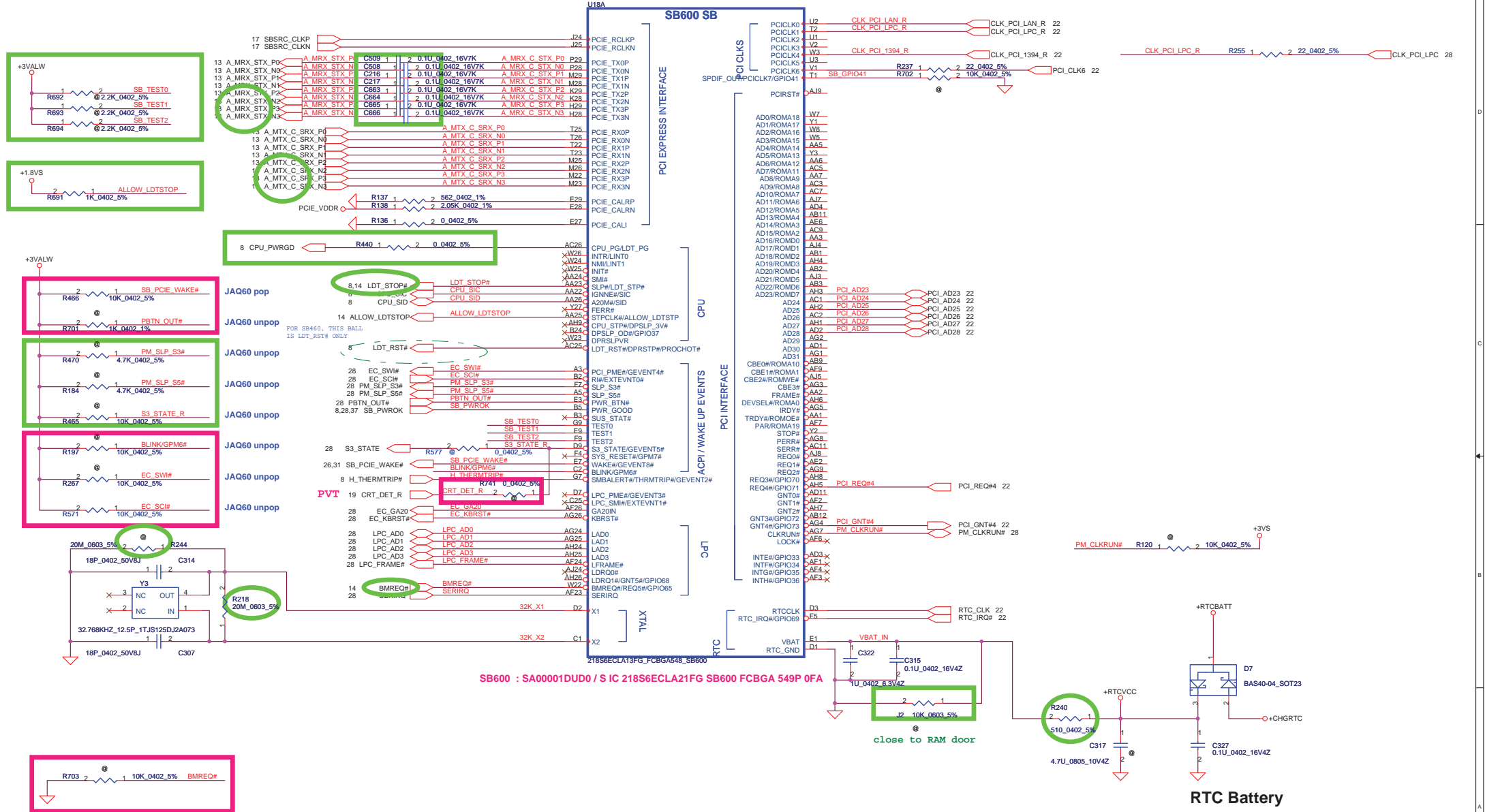


EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



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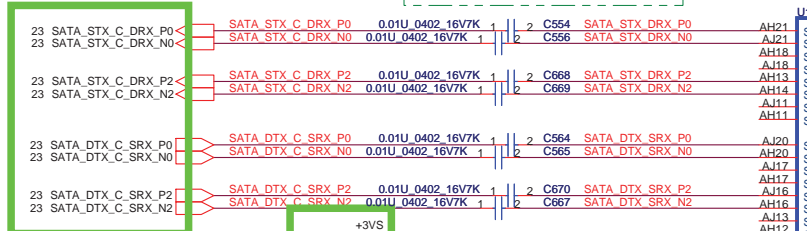


SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

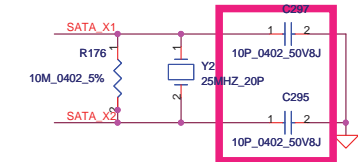
RTC Battery

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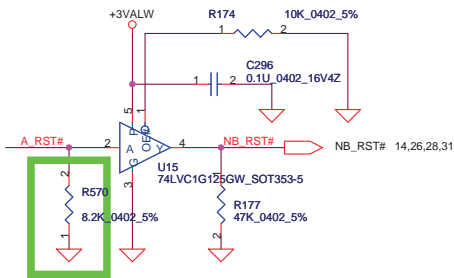
PLACE SATA AC COUPLING
CAPS CLOSE TO SB460



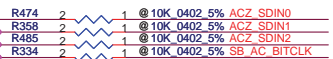
Change Y2 from SJ125POM780(KDS) as
SJ125POM200(TXC) (2006/08/31)



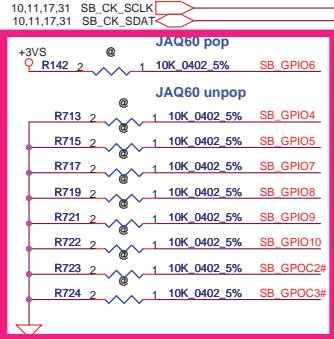
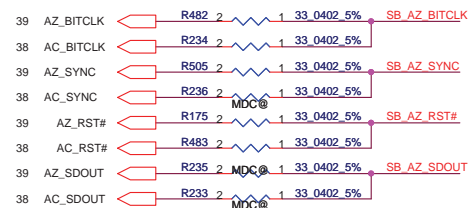
2005/12/30 Change net to +3VALW



2006/05/26 Change as SA411250200 from SA411250130



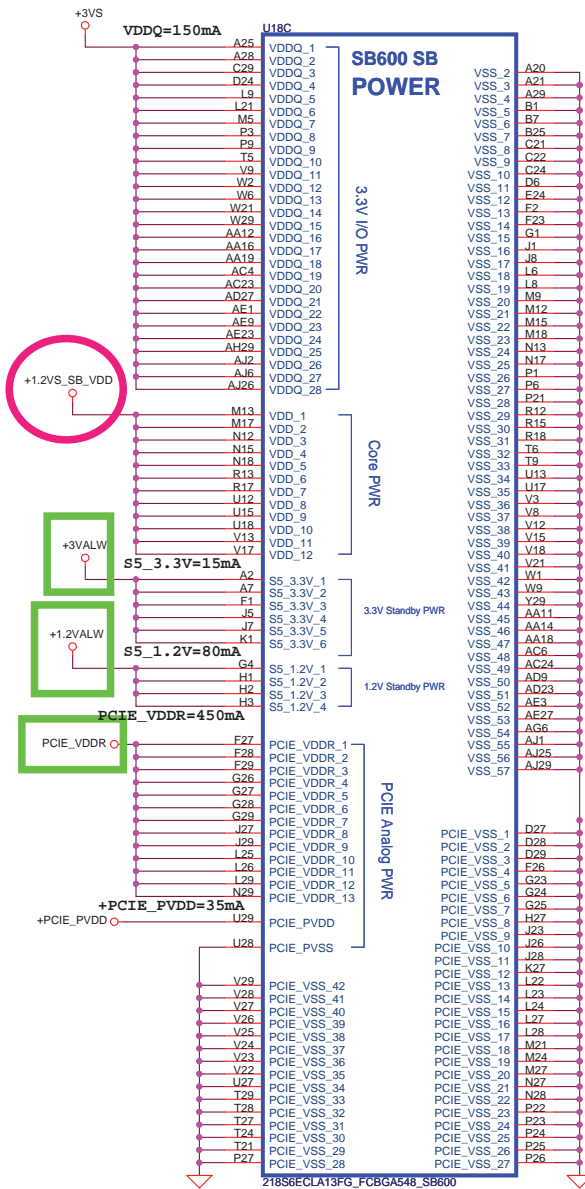
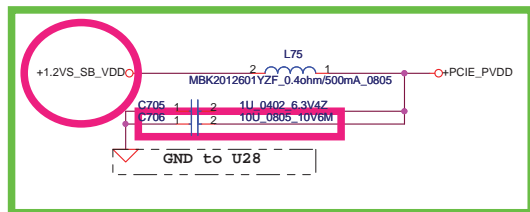
SB600 A21 and newer: Made provision for an external
10-kohm 5% pull-down resistor, not installed by default.



SB600 : SA00001DUD0 / S IC 21856ECLA21FG SB600 FCBGA 549P 0FA

Security Classification		Compal Secret Data	
Issued Date	2005/03/08	Deciphered Date	2006/03/08
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SB600-SATA/GPIO/USB/AUDIO			
Size	Document Number	Rev	
Custord	KAW60 LA-4661P	2.0	
Date:	Friday, July 25, 2008	Sheet	19 of 50

Security Classification		Compal Secret Data		Title SB600-PWR & GND I	
Issued Date	2005/03/08	Deciphered Date	2006/03/08		
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				Date: Thursday, July 24, 2009	Rev 2.0



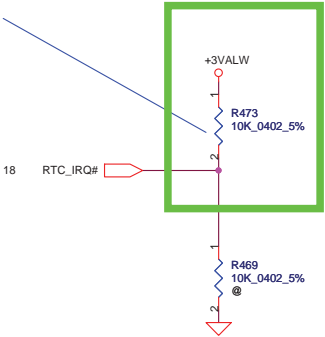
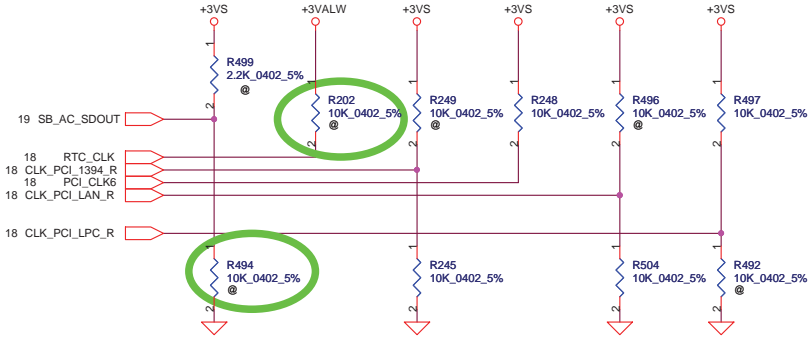
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Security Classification		Compal Secret Data		Title SB600-PWR & GND II		
Issued Date	2005/03/08	Deciphered Date	2006/03/08			
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				Custom	KAW60 LA-4661P	
				Date		Thursday, July 24, 2008

REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED

NOTE: R473 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB600
TO KEEP THE INPUT FROM FLOATING.



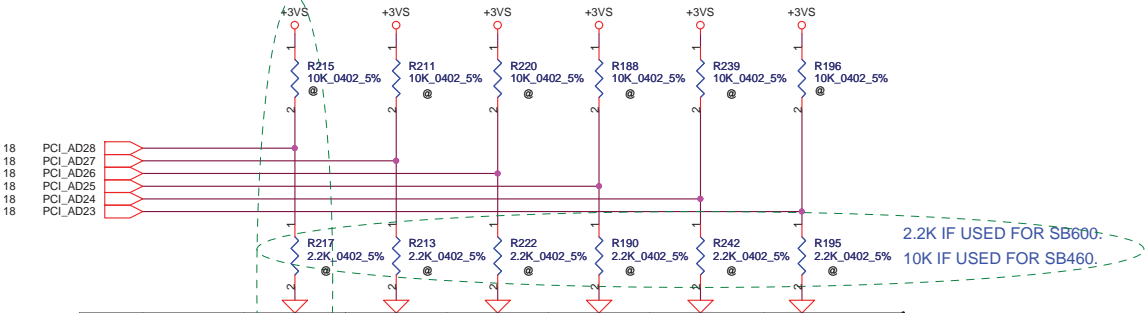
SB460 ONLY

PULL HIGH	ACPWON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

PULL HIGH	AC_SDOOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	SB600		SB460	
	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	PCI_LAN_R	PCI_LPC_R	PCI_LAN_R	PCI_LPC_R
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM DEFAULT		ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

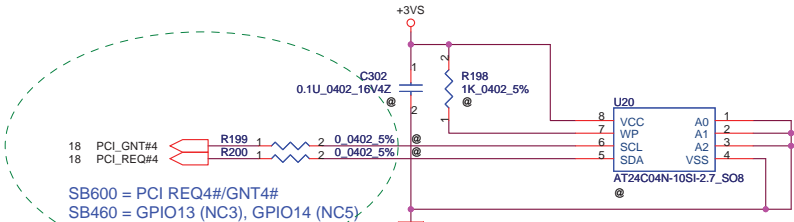


	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

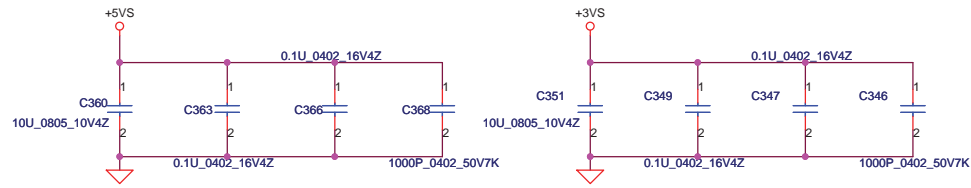


SB PCIE EEPROM STRAPS

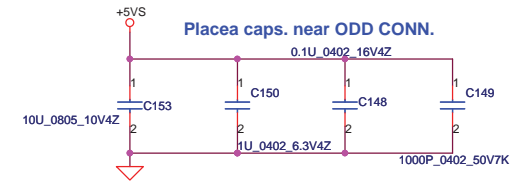
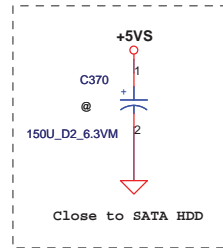
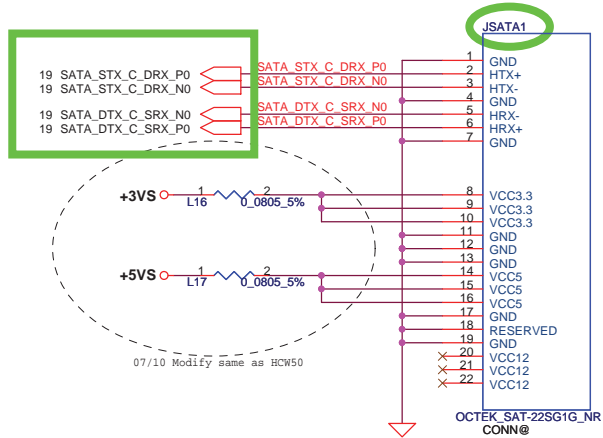
SB460 ONLY

SB600 ONLY

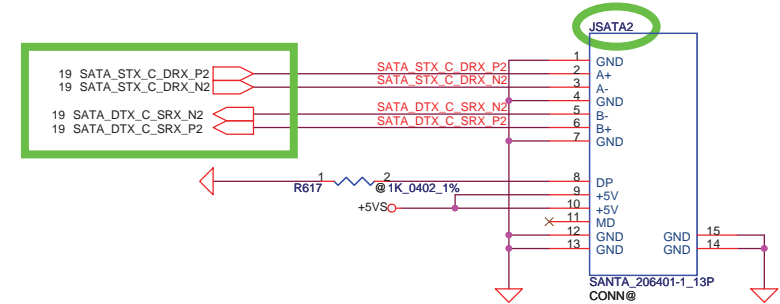
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	Title	SB600-STRAPS	
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					KAW60 LA-4661P	2.0
				Date:	Friday, July 25, 2008	Sheet



SATA HDD CONN

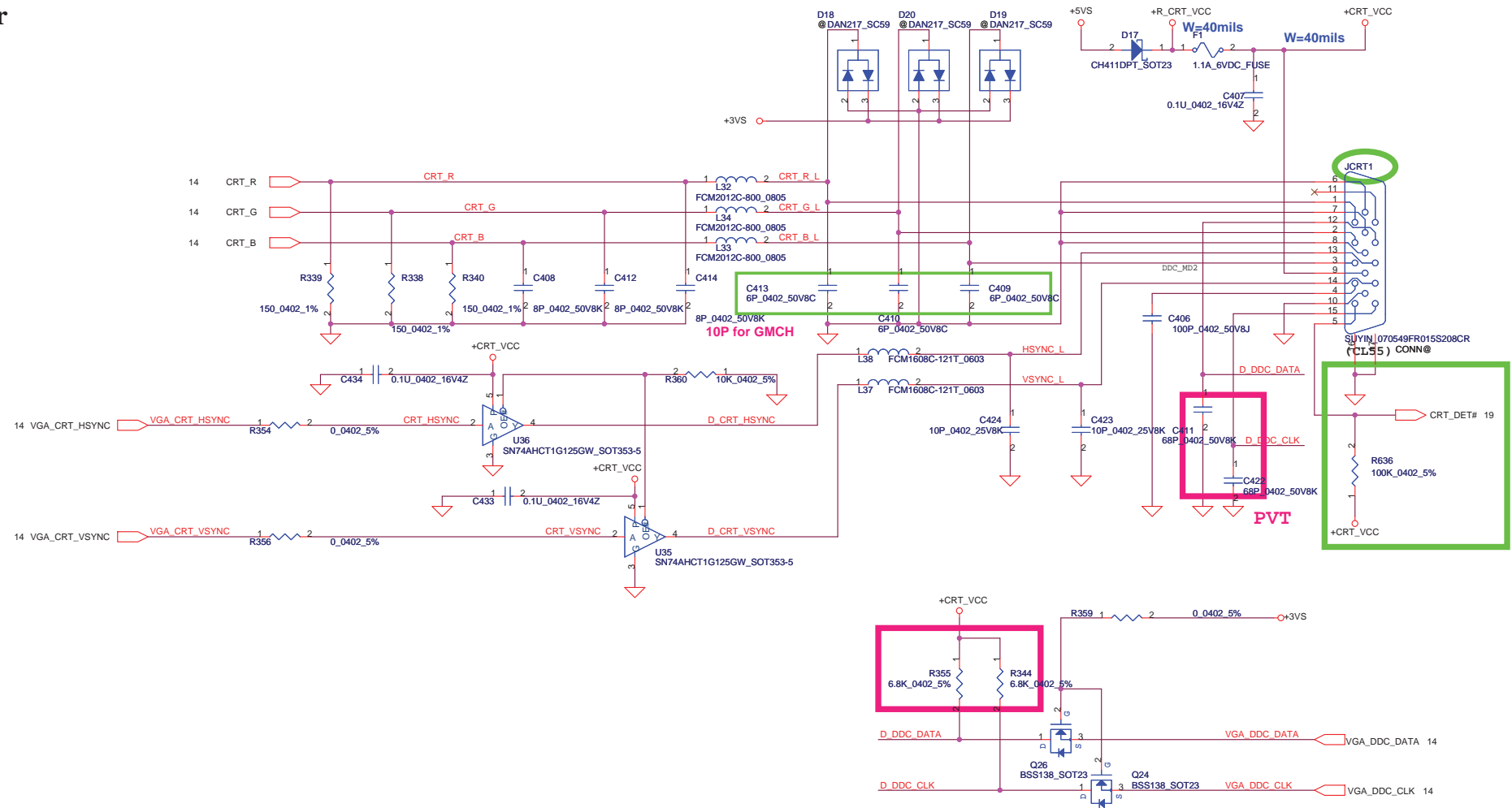


SATA ODD CONN



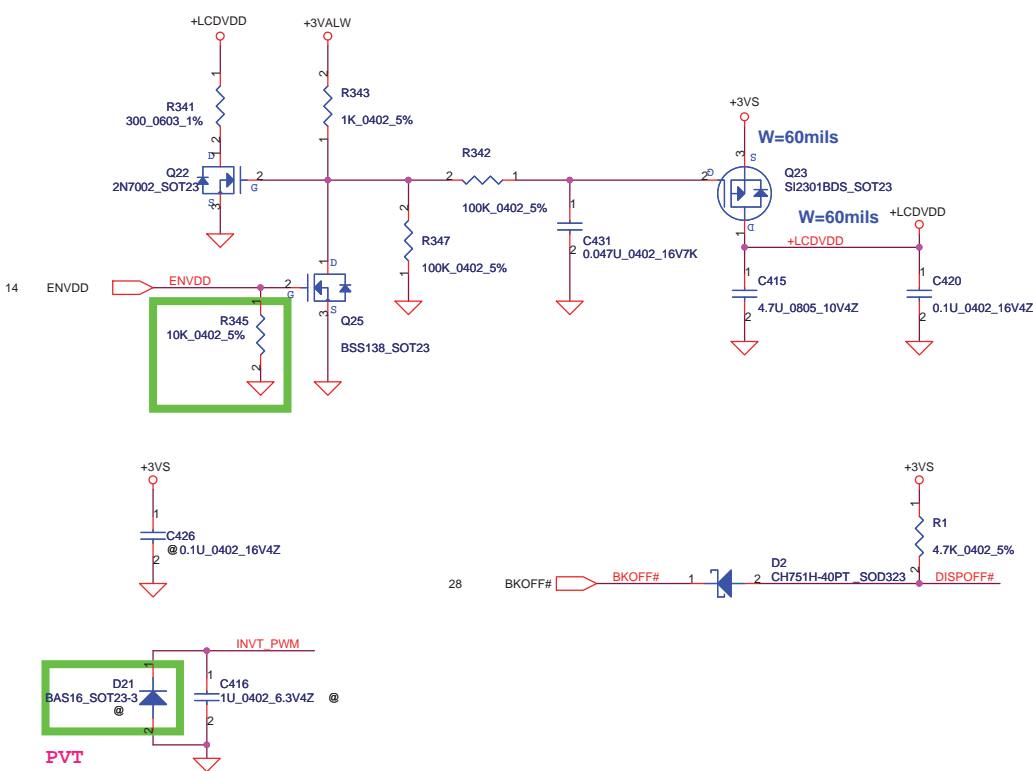
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	Size	HDD/CDROM
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				KAW60 LA-4661P	2.0
				Date	Friday, July 25, 2008
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CRT Connector

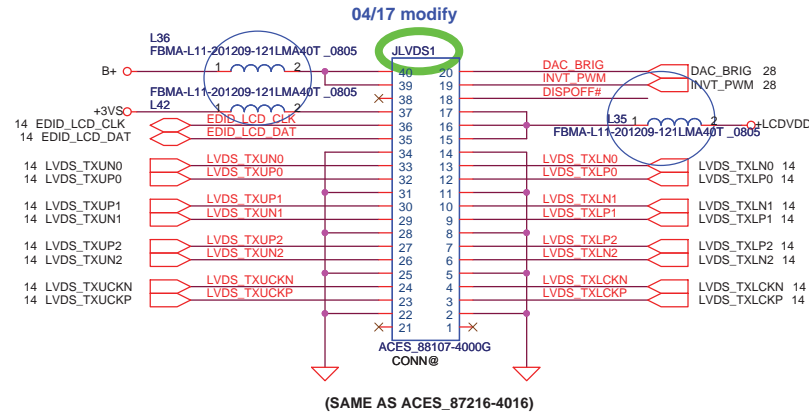


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						Size	Document Number			Rev	
						Custord	KAW60 LA-4661P			2.0	
						Date:	Tuesday, July 29, 2008		Sheet	24	of

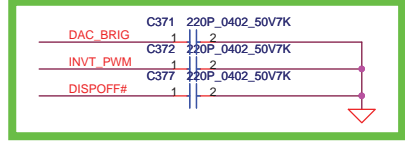
LCD POWER CIRCUIT



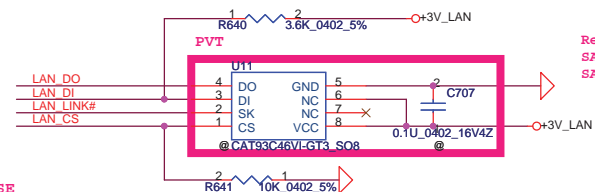
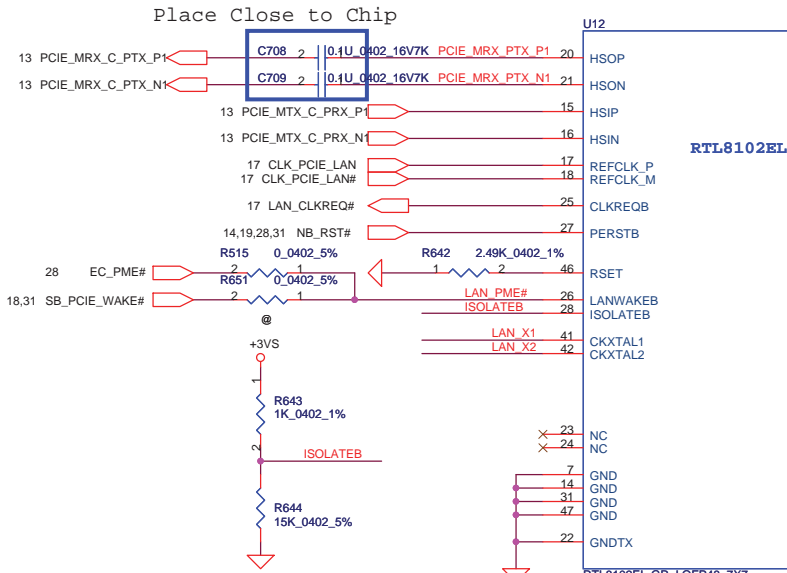
LCD/PANEL CONN.



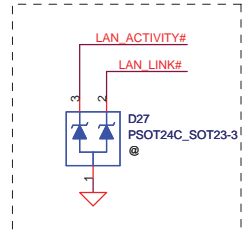
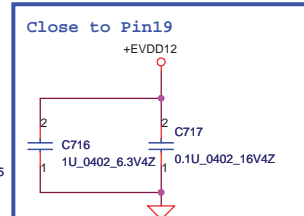
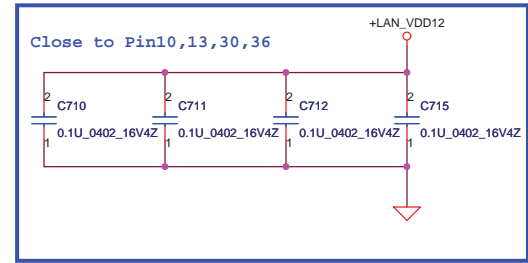
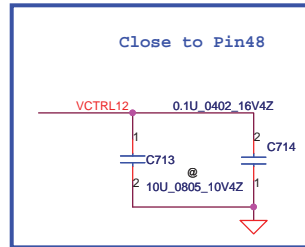
EMI



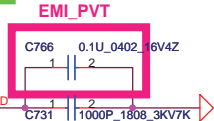
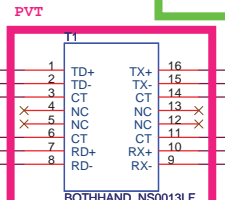
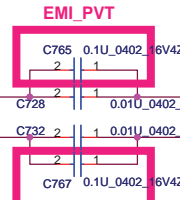
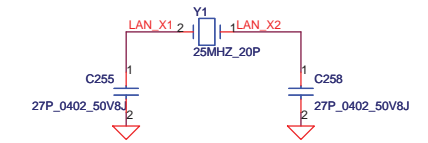
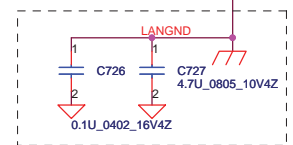
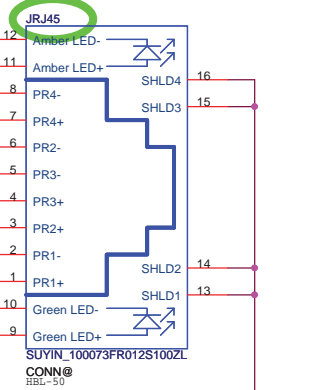
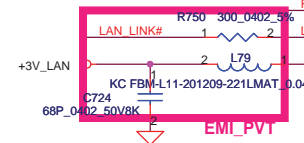
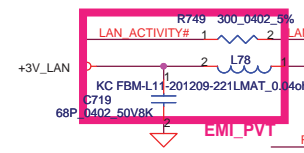
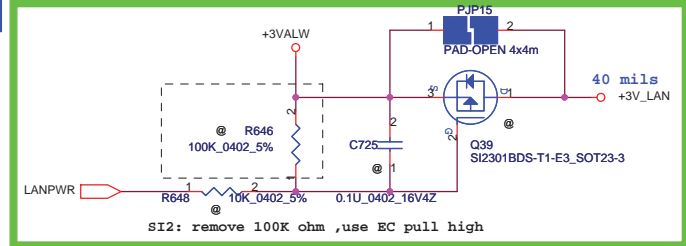
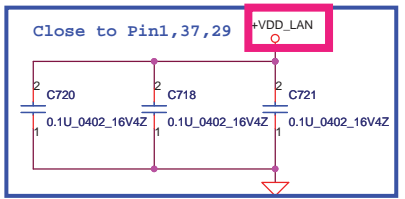
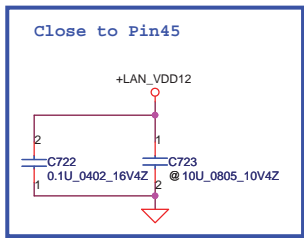
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Remove U11 & C707 (Embedded memory to replace ext. EEPROM)
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 SA093461070 / S IC EE 1K SO-8 I AT93C46-10SI-2.7 (EOL)



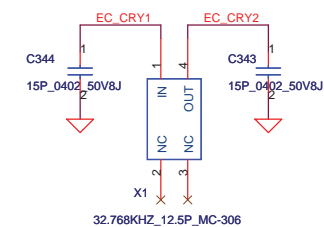
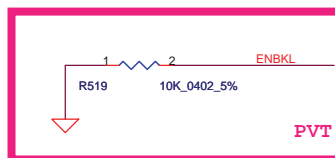
PV:Add ESD diode for EMI request



SP050003N00 S X'FORM_N8681680 LAN (MHPC , Not for ABO)
 SP050001210 S X'FORM_N80013LF LAN (BOTHAND)
 SP050001310 S X'FORM_LF-H80P-1 COUPLING (lankom)
 SP050004L00 S X'FORM_HD-024A 10/100 PC CARD LAN (TAIMAG)

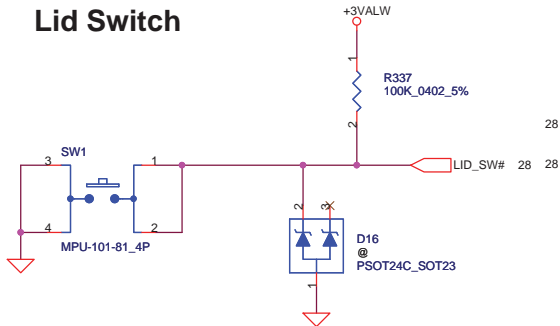
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								LAN RTL8102EL & RJ45					
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										KAW60 LA-4661P			
								Date:		Friday, July 25, 2008		Sheet 26 of 50	

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<table><tr><td colspan="2">Security Classification</td><td colspan="2">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td colspan="2">Issued Date</td><td colspan="1">2005/07/29</td><td colspan="1">Deciphered Date</td><td colspan="1">2006/07/29</td><td colspan="1">Title</td></tr><tr><td colspan="5">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td><table><tr><td>Size B</td><td colspan="3">Document Number KAW60 LA-4661P</td><td>Rev 2.0</td></tr><tr><td>Date: Tuesday, June 17, 2008</td><td colspan="1">Sheet 27</td><td colspan="1">of 50</td><td colspan="2"></td></tr></table></td></tr></table>					Security Classification		Compal Secret Data		Compal Electronics, Inc.		Issued Date		2005/07/29	Deciphered Date	2006/07/29	Title	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					<table><tr><td>Size B</td><td colspan="3">Document Number KAW60 LA-4661P</td><td>Rev 2.0</td></tr><tr><td>Date: Tuesday, June 17, 2008</td><td colspan="1">Sheet 27</td><td colspan="1">of 50</td><td colspan="2"></td></tr></table>	Size B	Document Number KAW60 LA-4661P			Rev 2.0	Date: Tuesday, June 17, 2008	Sheet 27	of 50		
Security Classification		Compal Secret Data		Compal Electronics, Inc.																												
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Size B	Document Number KAW60 LA-4661P			Rev 2.0																												
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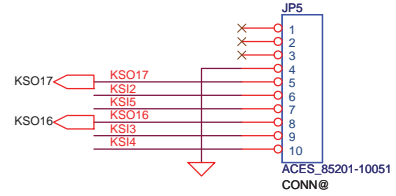


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Issued Date	2007/5/18	Deciphered Date	2008/5/18	Title		
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				Size Custom	Document Number	Rev
				KAW60 LA-4661P		0.2
Date:				Friday, July 25, 2008	Sheet	28 of 50

Lid Switch

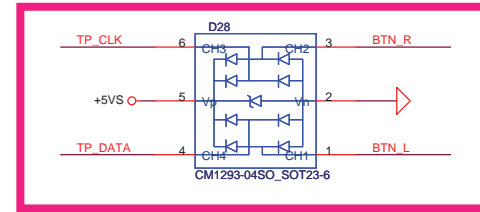


W/O media board (LS2921P)

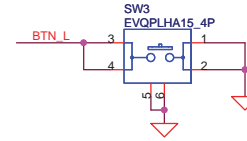


	KSO16	KSO17
KSI2	PLAY	
KSI3	STOP	VOL_UP
KSI4	NEXT	VOL_DOWN
KSI5	REV	ARCADE_TV

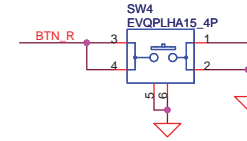
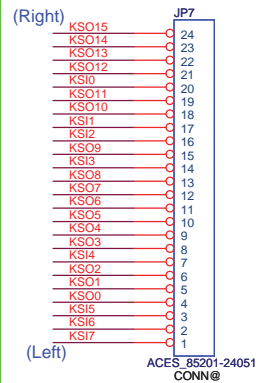
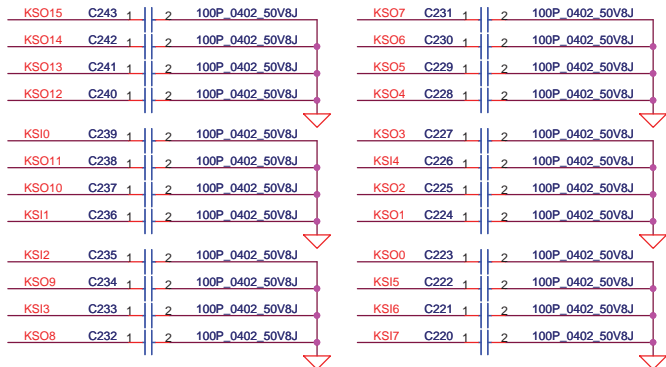
PVT



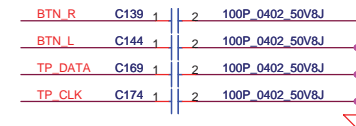
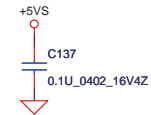
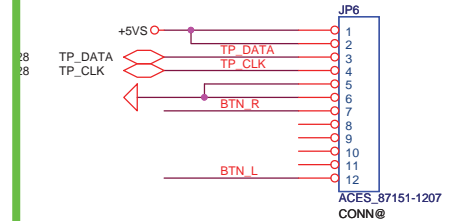
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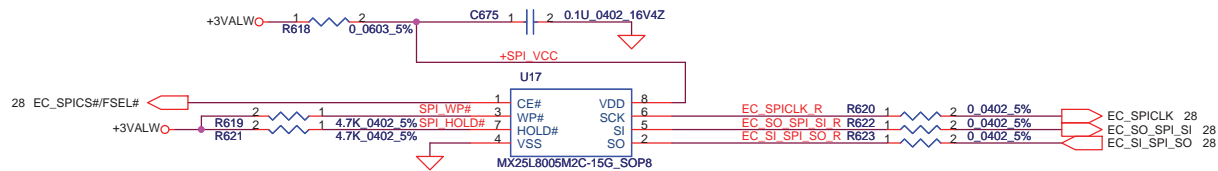
Right

**INT_KBD Conn.**

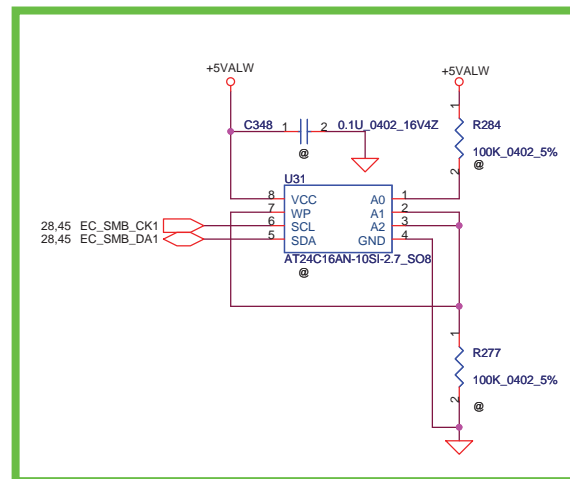
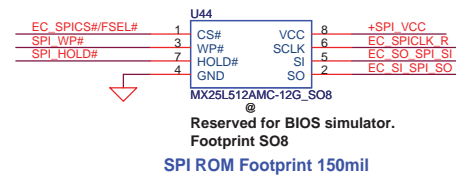
To TP/B Conn.



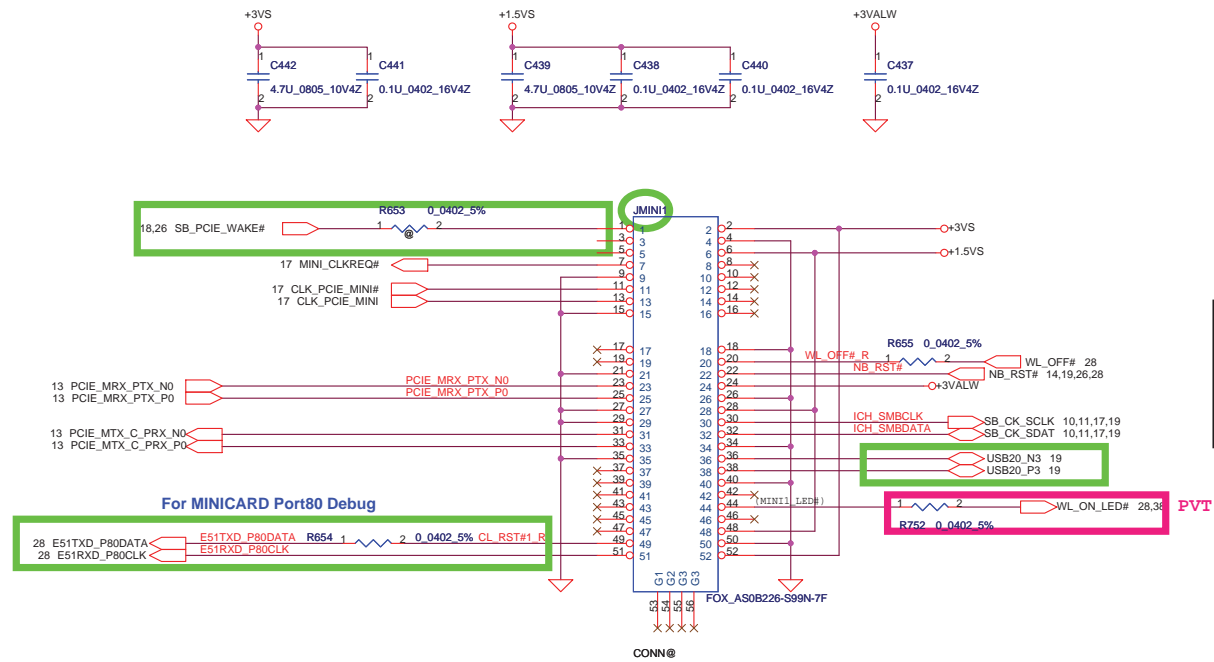
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SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

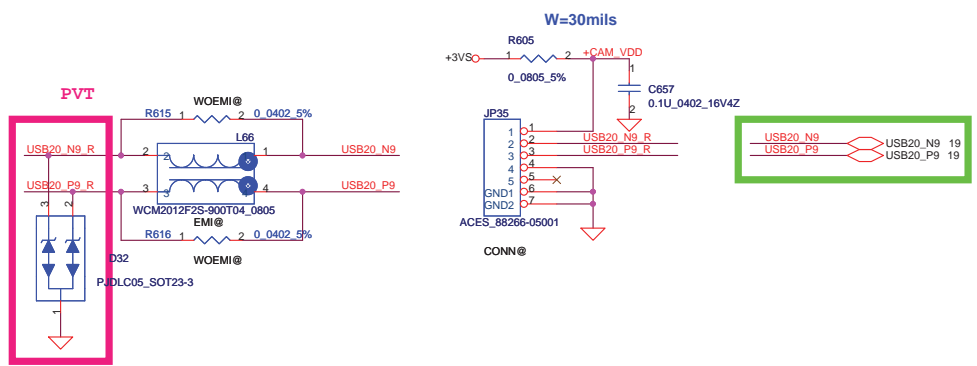


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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

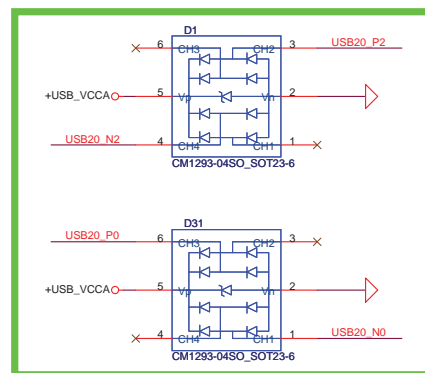
Camera



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A		B		C		D		E	
1									
2									
3									
4									

A		B		C		D		E	
1									
2									
3									
4									



A

A		B		C		D		E	
1									
2									
3									
4									

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Power ON Circuit

28,41 VLDT_EN

R100 47K_0402_1%

C203 1U_0603_10V4Z

PVT

U10A SN74LVC14APWR_TSSOP14

U10B SN74LVC14APWR_TSSOP14

U10E SN74LVC14APWR_TSSOP14

U10F SN74LVC14APWR_TSSOP14

R104 10_0402_5%

R105 100K_0402_5%

R108 10_0402_5%

R109 10_0402_5%

R110 10K_0402_5%

R111 10K_0402_5%

R112 100K_0402_1%

R113 180K_0402_5%

C204 1U_0805_25V4Z

SB_PWRGD 8,18,28

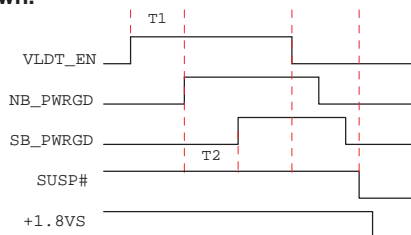
NB_PWRGD 14,28

2006/02/22 Change R100 to 47K

note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms. SUSP# goes to low after SB_PWRGD goes to low for power down.

2006/02/22 Change R100 to 47K

**note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.**



TOP Side

3V_ALW

R281 100K_0402_5%

J3 10K_0603_5%

J4 10K_0603_5%

Bottom Side

38 ON/OFFBTN#

ON/OFFBTN#

D10 CHN202UPT_SC70

28 ON/OFF 28

51ON# 42

28 EC_ON

EC_ON

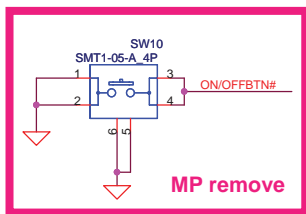
R290 10K_0402_5% <BOM Structure>

2N7002_SOT23 Q17

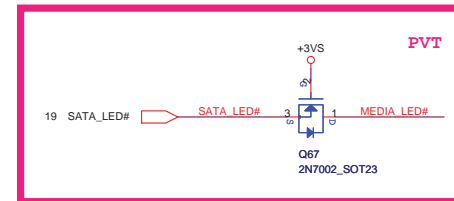
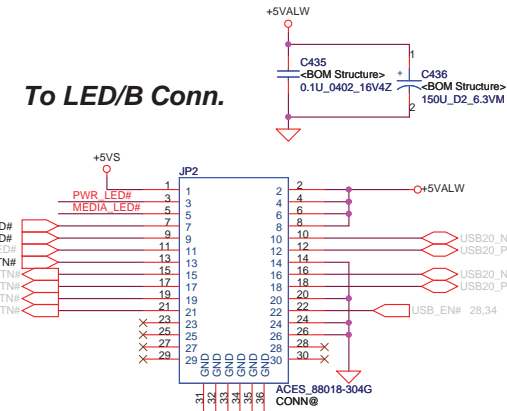
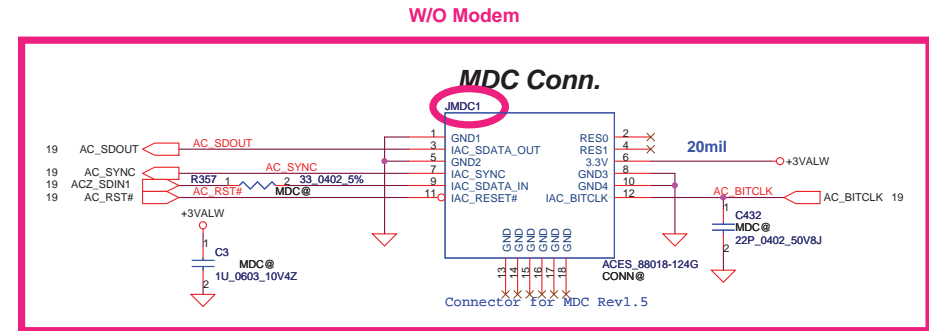
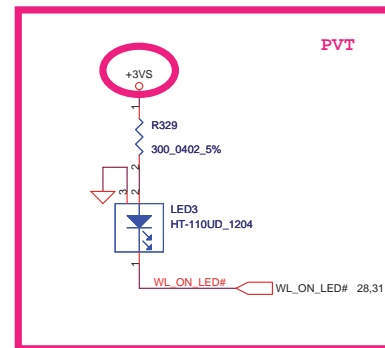
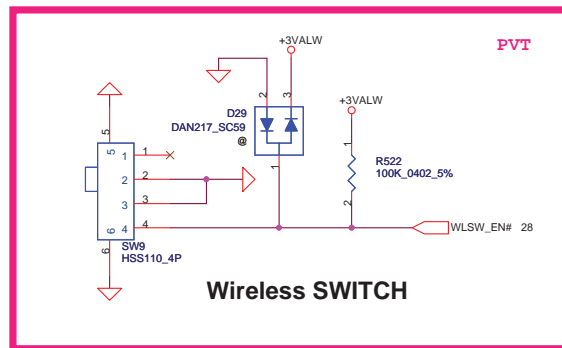
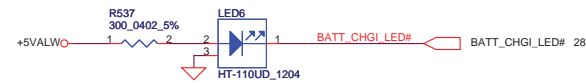
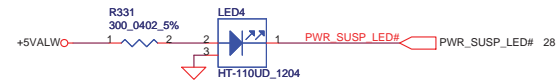
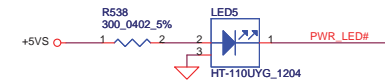
C358 1000P_0402_50V7K

D11 RLZ20A_LL34

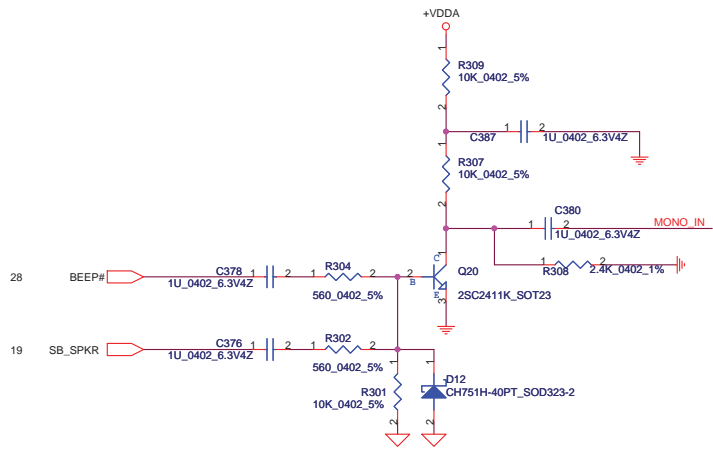
move



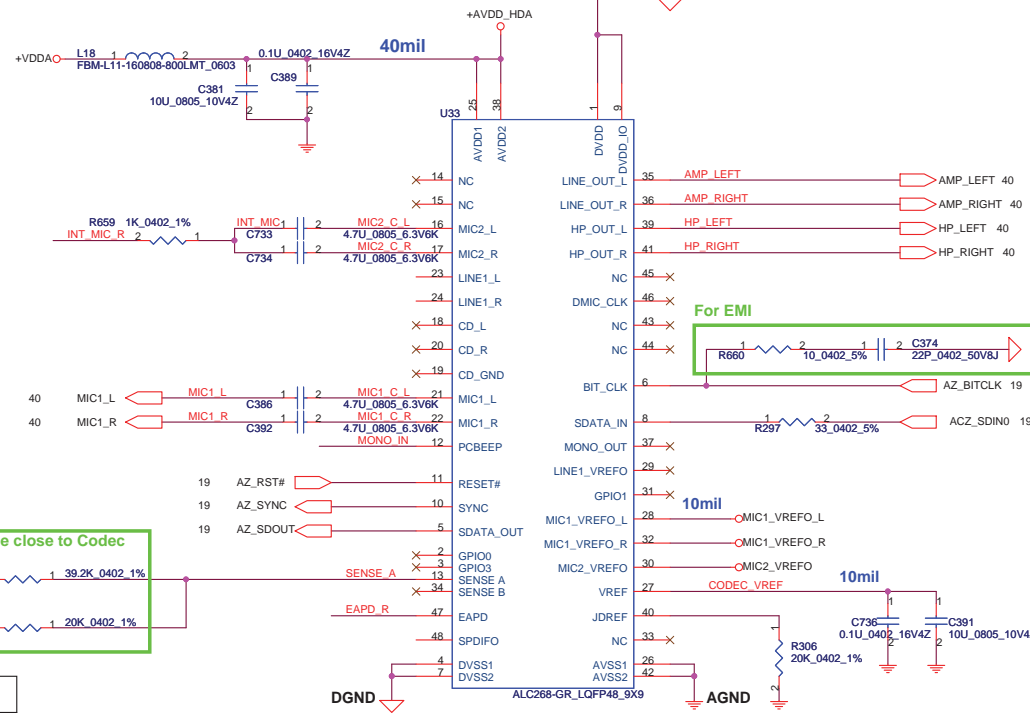
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Issued Date	2005/03/08	Deciphered Date	2006/03/08	Title	PWR_OK/ PWR BTN
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title MDC / LED / SW			
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				Date:	Friday, July 25, 2008	Sheet	38 of 50

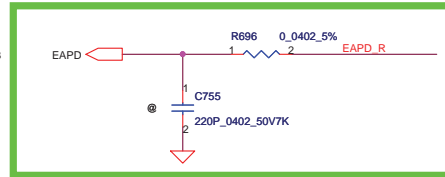


HD Audio Codec



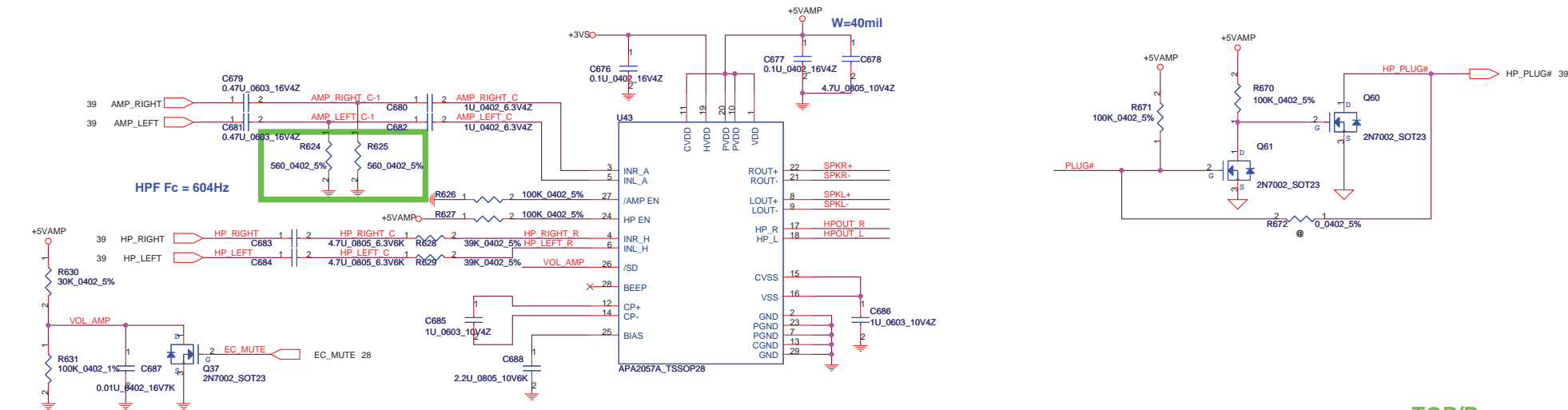
Place close to Codec

For EMI request

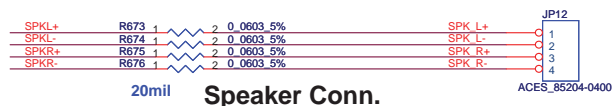


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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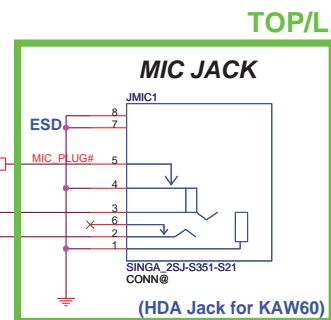
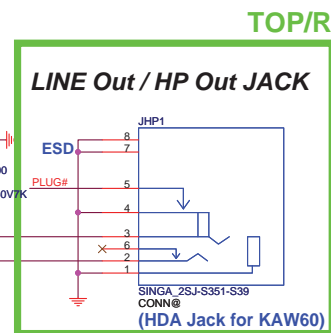
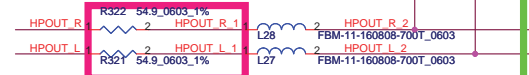


Gain= 14dB

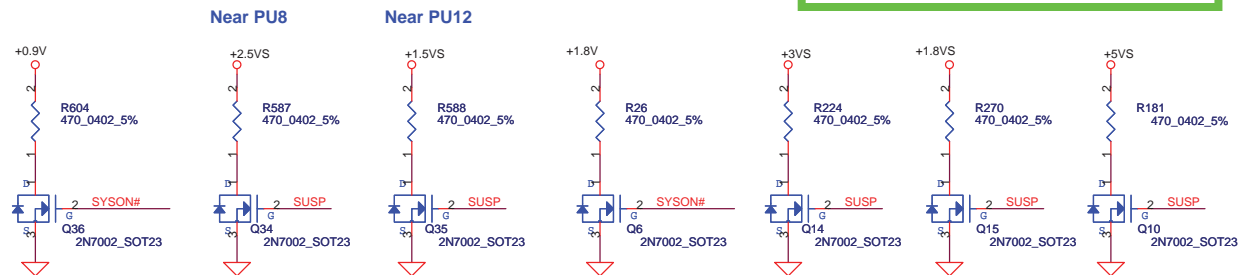
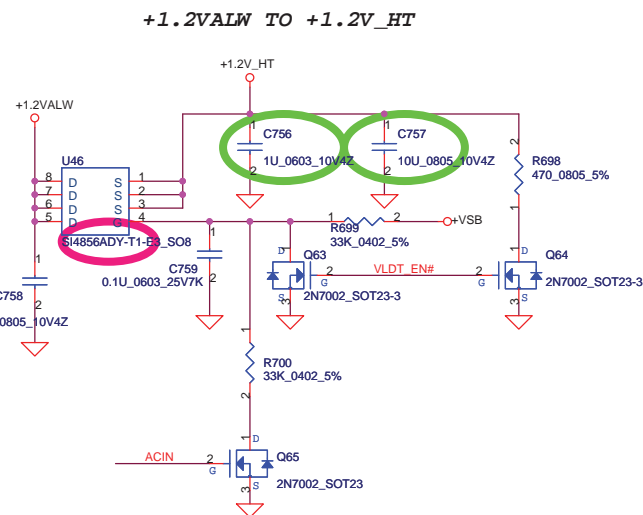
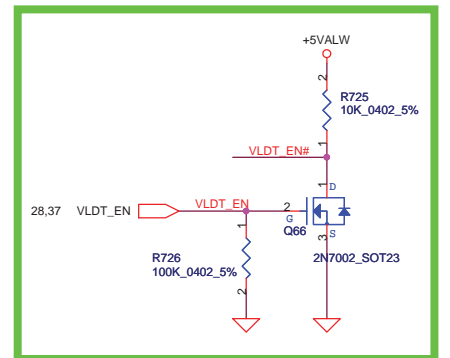
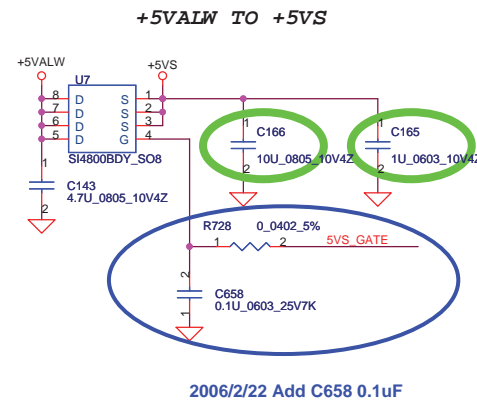
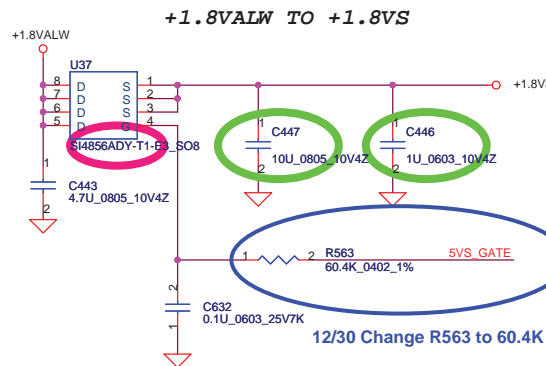
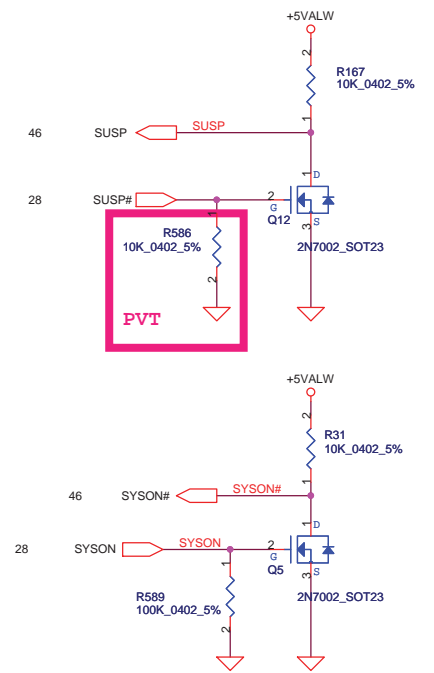
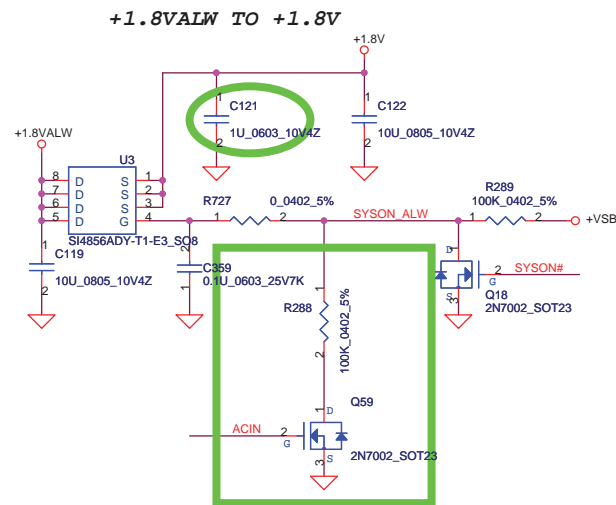


Speaker Conn.

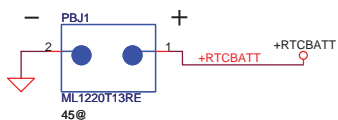
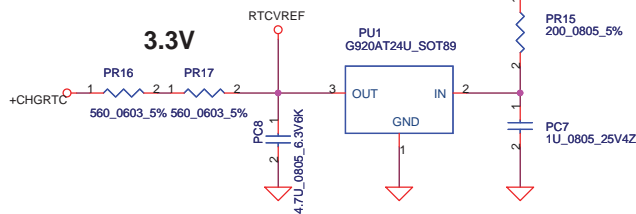
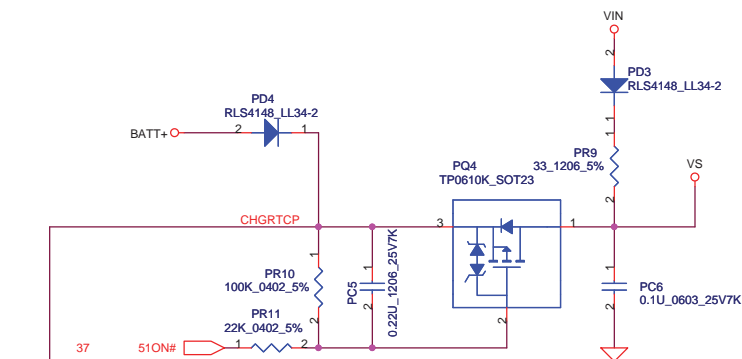
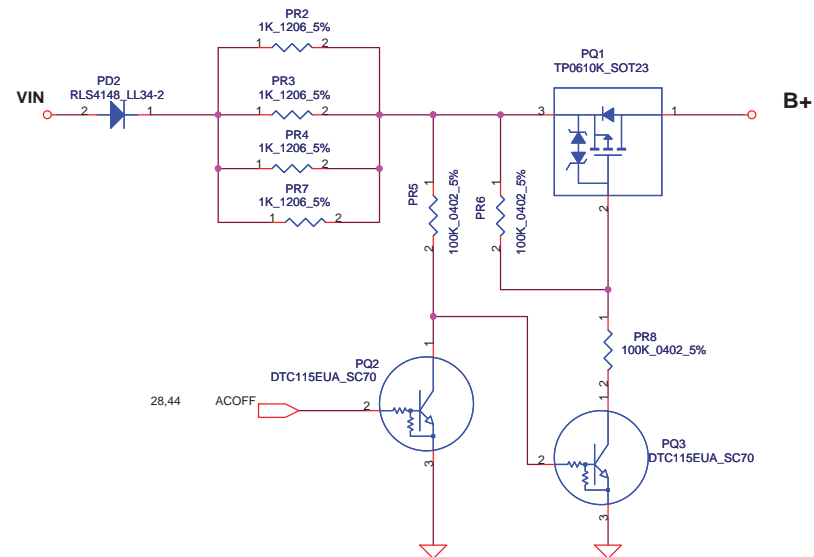
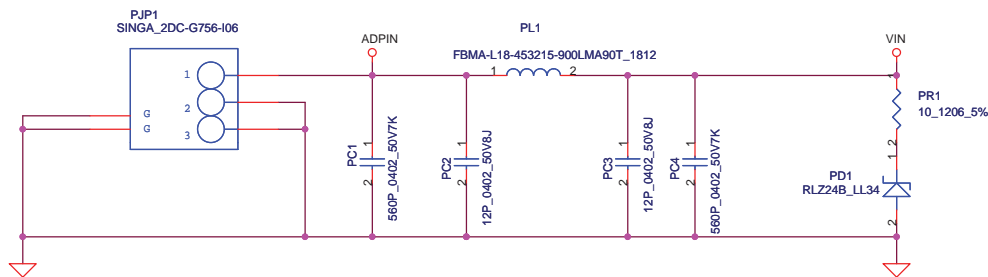
FSOV_Change 75 to 54.9 ohm



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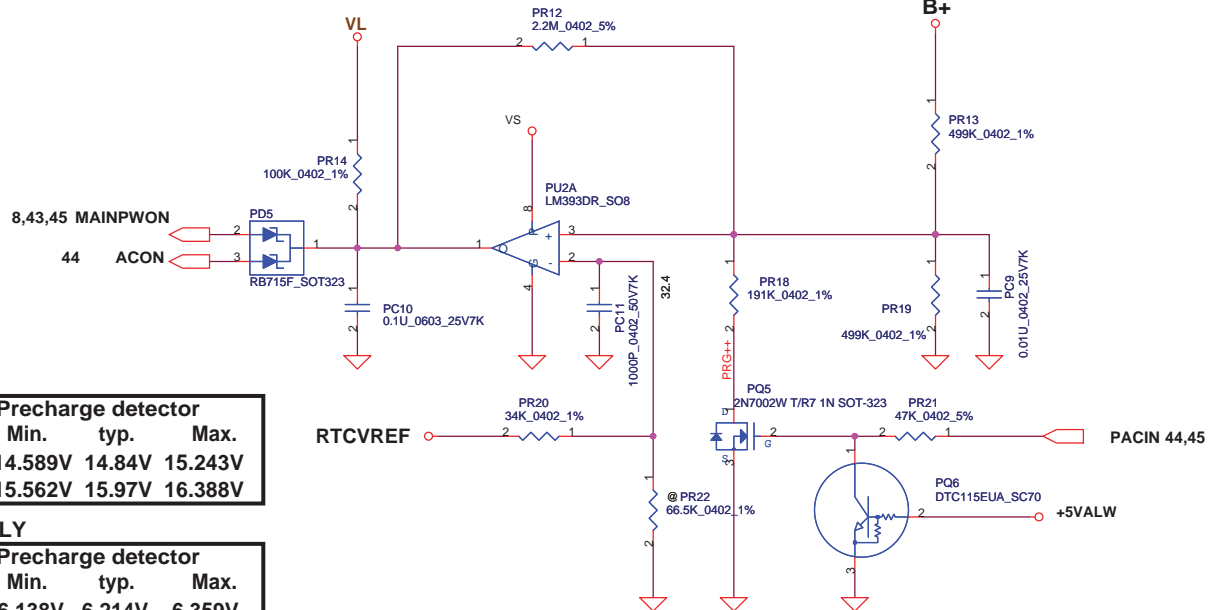


ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

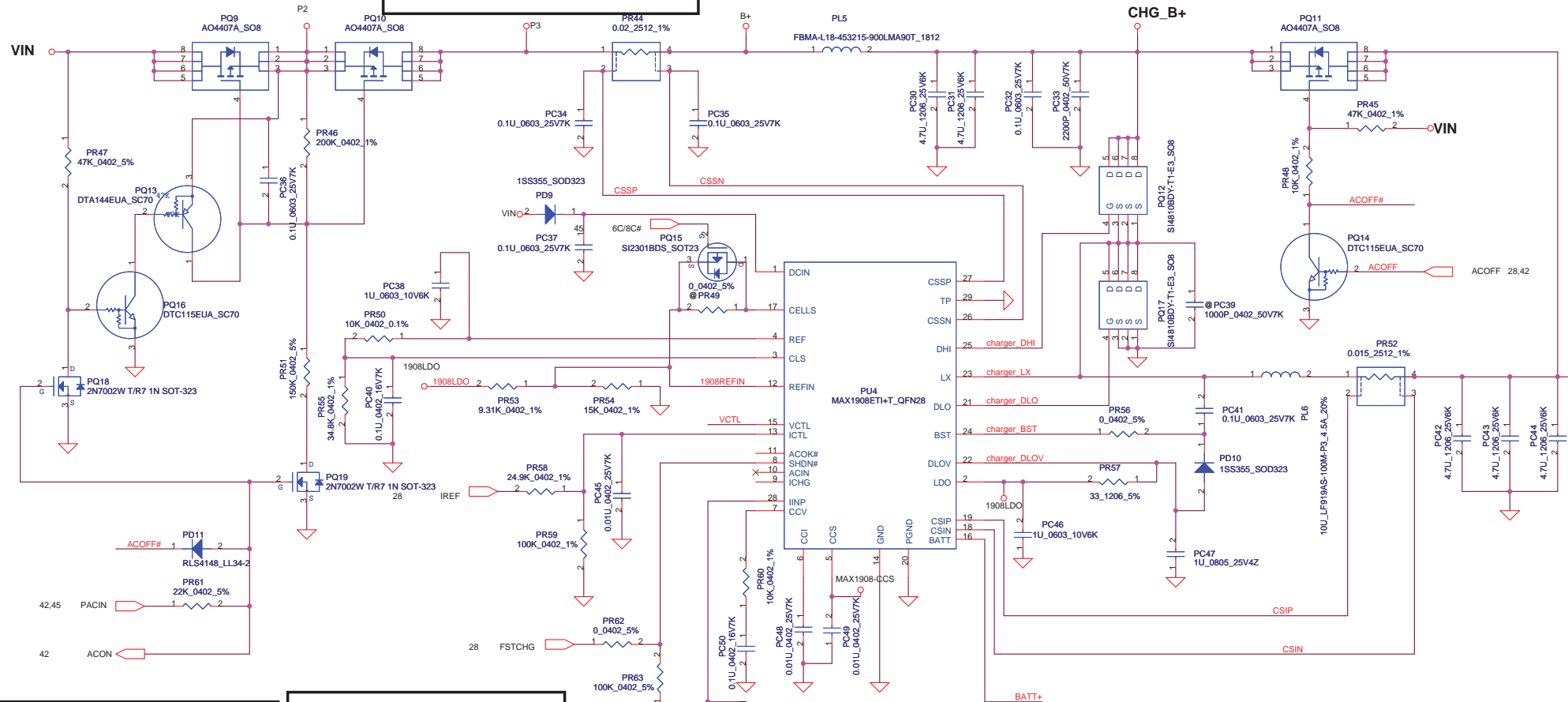
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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I_{adp}=0~2.912A(65W)

CP Point:
85% CP Point, $3.42A \times 0.85 = 2.907A \sim 2.912A$
Input = $(34.8K/44.8K) \times (75/20) = 2.912A$



Charger ADJ	Calibrate#	PR170	PR173
4.0V	L	@	@
4.1V	L	665K	221K
4.2V	H	@	@

```
Vrefin=V1908LDO*(15K/(9.31K+15K))
=5.4V*(15K/(9.31K+15K))=3.331V

Vvctl=3.331*(221K/(221K+665K))=0.83087V

Vbatt=CELLS*(4+(0.4*(Vvctl/Vrefin)))
=3*(4+(0.4*(0.83087/3.331)))=12.29v
```

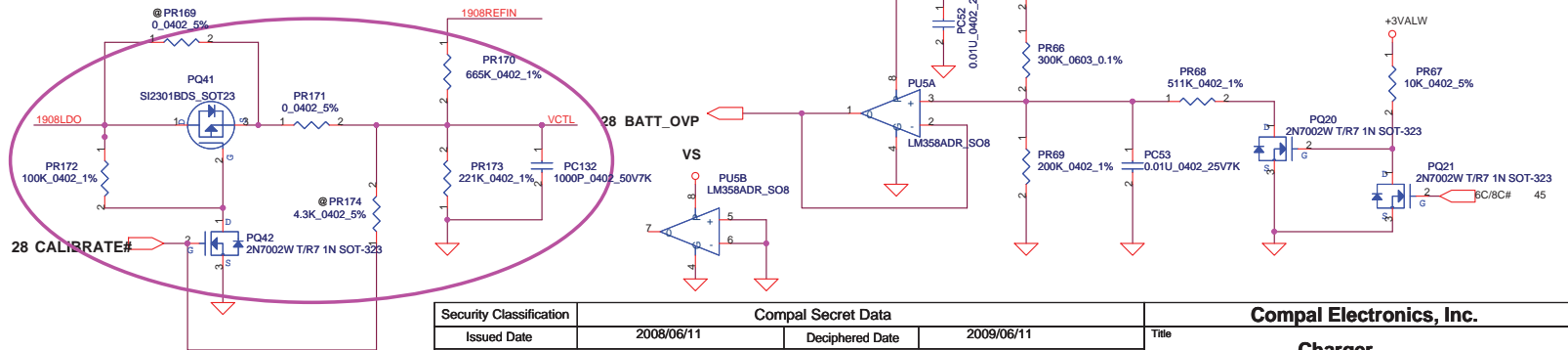
```
IREF=0.832*Icharge
IREF=0.73~3.3V
```

2P3S:4400mAH
0.8C=3.52A

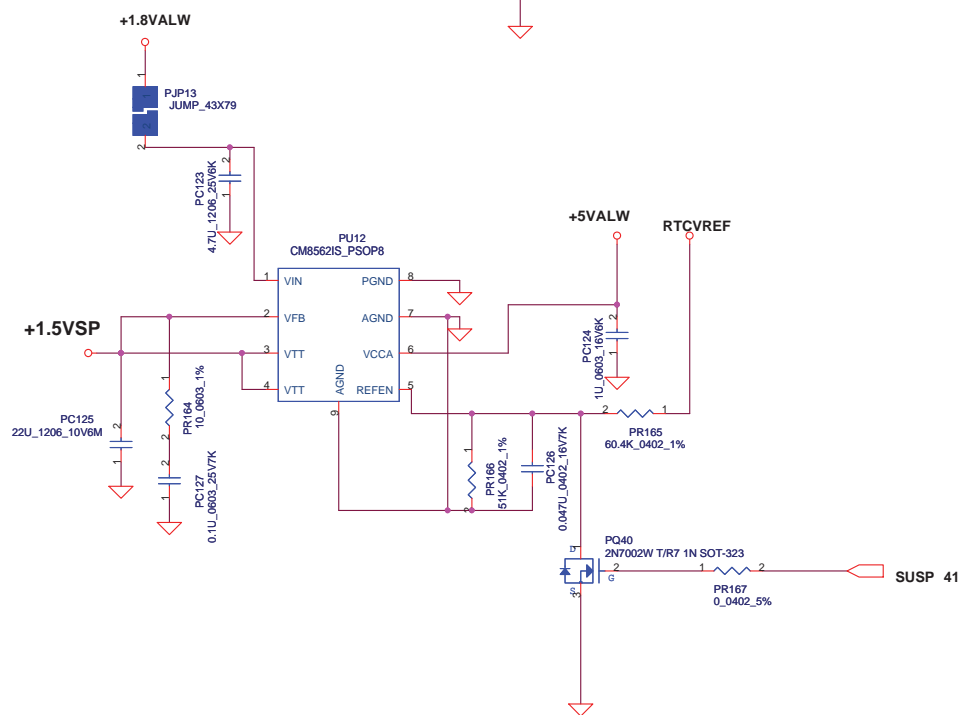
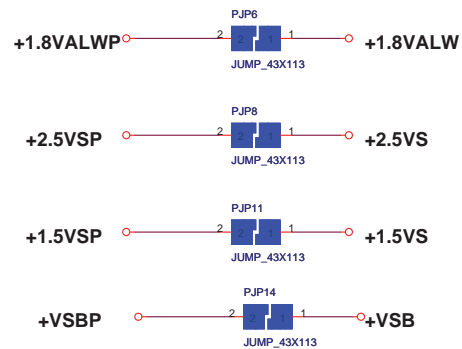
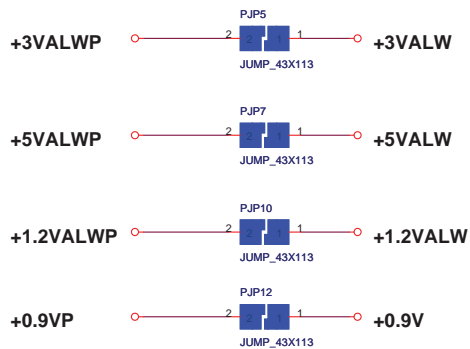
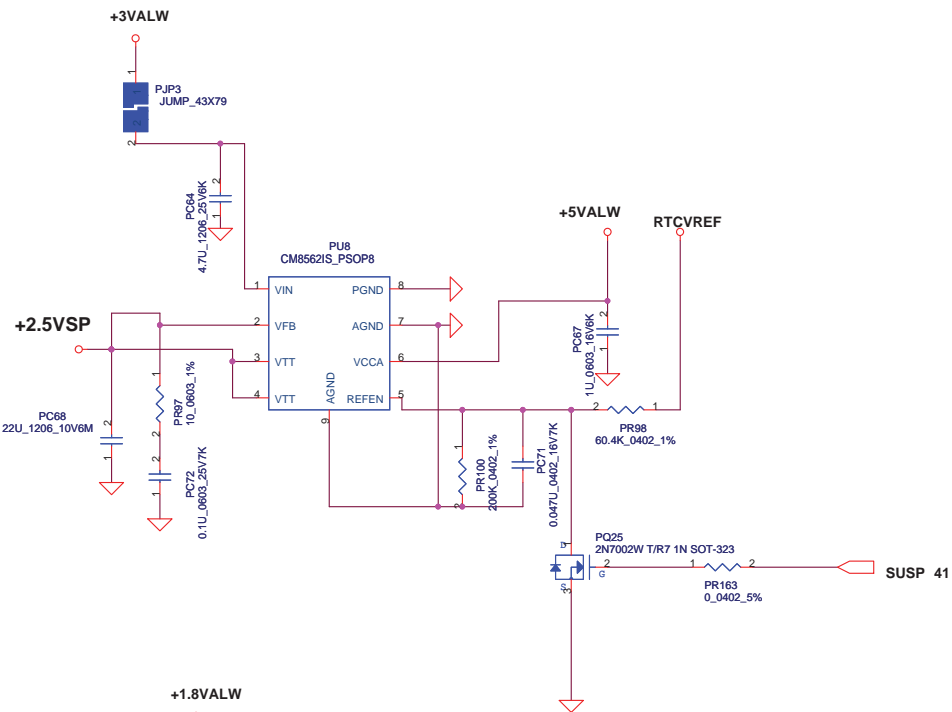
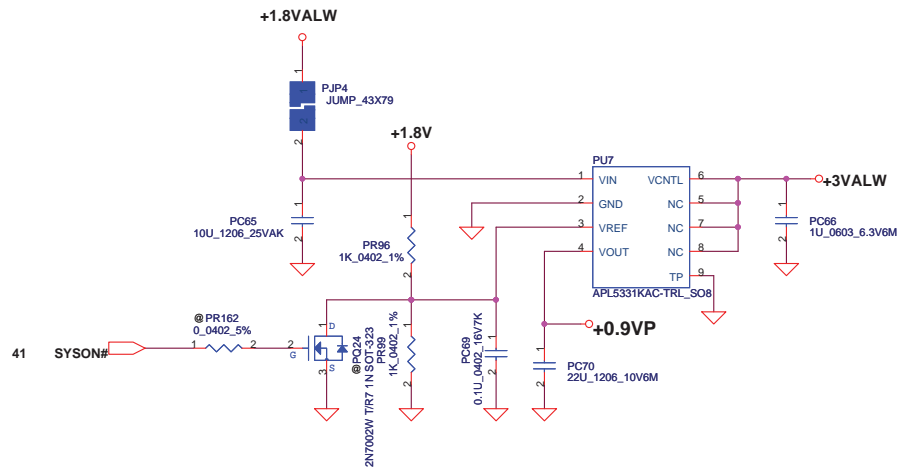
```
OVP-Voltage:
LI-3SBattery Pack=13.5V---BATT-OVP=2.0061V
Battery-OVP=0.1486*BATT+
```

$$V_{batt} = CELLS * (4V + (0.4 * (V_{vctl} / V_{refin})))$$

Charge voltage
3S CC-CV MODE : 12.6V



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				+0.9VSP/+1.5VSP/+2.5VSP	
				Size	Document Number
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	material issue.	Change to currently design	0.1	44	Change PQ9, PQ10, PQ11 from SB944070000(S TR AO4407 1P SO8 W/D) to SB00000DL00(S TR S TR AO4407A 1P SO8)	08,07/22	to PVT
2	material issue.	Change to currently design	0.1	48	Change PQ31 and PQ35 from SB578400080(S TR SI7840-T1 -E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK SO8)	08,07/22	to PVT
3	material issue.	AO4916 will be EOL, change to AO4932	0.1	43	Change PQ7 and PQ8 from SB000002W80(S TR AO4916 2N SO8) to SB00000BG00(S TR AO4932 2N SO8)	08,07/22	to PVT
4	BOM error	BOM error	0.1	48	Change PR141 from SD014200180(S RES 1/10W 2K 0603 1%) to SD014432180(S RES 1/10W 4.32K 0603 1%)	08,07/22	to PVT
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Security Classification		Compal Secret Data		Title	
Issued Date	2008/06/11	Deciphered Date	2009/06/11	PIR(PWR)	
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PHASE	PAGE	MODIFICATION LIST	PURPOSE
PVT	P.19 & 24	Update CRT_DET & CRT_DET# net name	NA
	P.18 & 19	Change CRT_DET from GPIO61 to GPIO0 & reserved R741 , R742 , R743	For ACER AP test CRT detect feature
	P.20	Remove L71 , C694 & C697	For +3Vs (1.5V) , +5Vs (0.388V) , +1.8Vs (0.154V) on S5 leakage issue
	P.28	Change R519 from 100K to 10K	For RS690MC ENBKL had unexpected 3.3V pulse before normal display & white screen flash symptom appear
	P.14	Reserved U48 , U49 , R744 , R745 , R746 , R747 , C763	For RS690MC ENBKL , ENVDD if had unexpected 3.3V pulse before normal display
	P.28 & 31	Modify WL_ON_LED# from KB926 to JMINI1 control	WL LED activity behavior controlled by wireless mini card itself
	P.38	Update SW9 Footprint & P/N	NA
	P.41	Change R586 from 100K to 10K	For Susp# had 3V level glitch when G3 to S5 (Plug AC in) & caused +5Vs /+3Vs had leakage immediately
	P.6	Change D4 as SC1BAS16000(S DIO BAS16PT SOT-23)	Sourcer recommend
	P.26	Change U11 as SA000019910(S IC EE 1K CAT93C46VI-GT3 SOIC 8P)	SA093461070 (S IC EE 1K SO-8 I AT93C46-10SI-2.7) EOL
	P.50	Change T1 as SP050001210 / S X'FORM_ NS0013LF LAN (BOTHHAND)	MHPC X'form part not for ABO , Sourcer recommend
	P.18	Delete R695,R179,R484 for SB_TEST pin	AMD reference schematic
	P.20	Reserved C764 (1u_0402)	AMD reference schematic & design guide
	P.38	Modify WL_LED power rail as +3Vs	NA
	P.28 & 38	Modify LED control of SATA drive from EC to SB (Add Q67)	EC(media_led#/pin86 , reference sata_led# from SB) control behavior abnormal
	P.17	Change C510 , C511 of 14.318MHz as 27P from 22P	NA
	P.37 & 25	Change D5 , D21 as SC1BAS16000	NA
	P.26	Add L77 , C765 , C766 , C767 & change R645 / R647 as L78 / L79 , reserved C719 , C724	EMI request
	P.31 & 34	Stuff L66 , L67 , L68 & remove R615 , R616 , R598 , R599 , R600 , R601	EMI request
	P.29	Stuff D28	ESD request
	P.6	Update net EN_DFAN1_R	NA
	P.6	Update JCPU1 PCB footprint as SOC127MM48X51-948	NA
	P.26	Add R749 , R750 (300ohm_0402)	For LAN external EEPROM program issue
	P.31	Add D32 (SCA00000A00)	ESD request
	P.28 & 31	Reserved R751 & R752	Reserved WL_LED controlled by EC (Navarrow project)
	P.24	Change C411 & C412 PN from SE081680k80 to SE071680J80	AP Code
	P.6	Change U1 as SA00001Z900 (S IC APL5605KI-TRL SOP 8P)	(SA009930010) S IC G993P1UF SOP 8P FAN LDO EOL
	P.9	Change C504 & C505 as SGA19331D10	(SGA19331D00) S POLY C 330U ESR15 , but need ESR9 (SGA19331D10)

ZZZ



PCB 06B LA-4661P REV0 M/B

LA4661MB Rev0 : DA600009Z00
LA4661MB Rev1 : DA6~
LA4661MB with Sub/B Rev1 : DAZ~

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	PIR-HW & Option Component	
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